ML2620 DATASHEET

(DIGEST)
Preliminary Version 2
Reviced on 31 August 2007

Contents

General Description

ML2620 is speaker amplifier with "LOUDNESS" of that technology can enlarge volume from small speaker without distortion and clipping noise. Since the LSI has ALC (Automatic Level Controller), it can enlarge volume, when audio signal is small. Besides, the LSI will protect speaker, when audio signal is too big. The LSI is the best speaker amplifier for mobile phone, DSC, portable TV and etc that play multi-media contents from built-in small speaker.

Features

1) CPU Interface
Support two mode
1-1) 2 wired serial interface
- 7bit address, slave address is fixed to "0011010"
- support Standard/Fast mode

1-2) 3 wired serial interface

2) OKI original "LOUDNESS" technology for volume enhancement

3) ALC (Auto level controller) embedded

4) Fade-in, Fad-out function

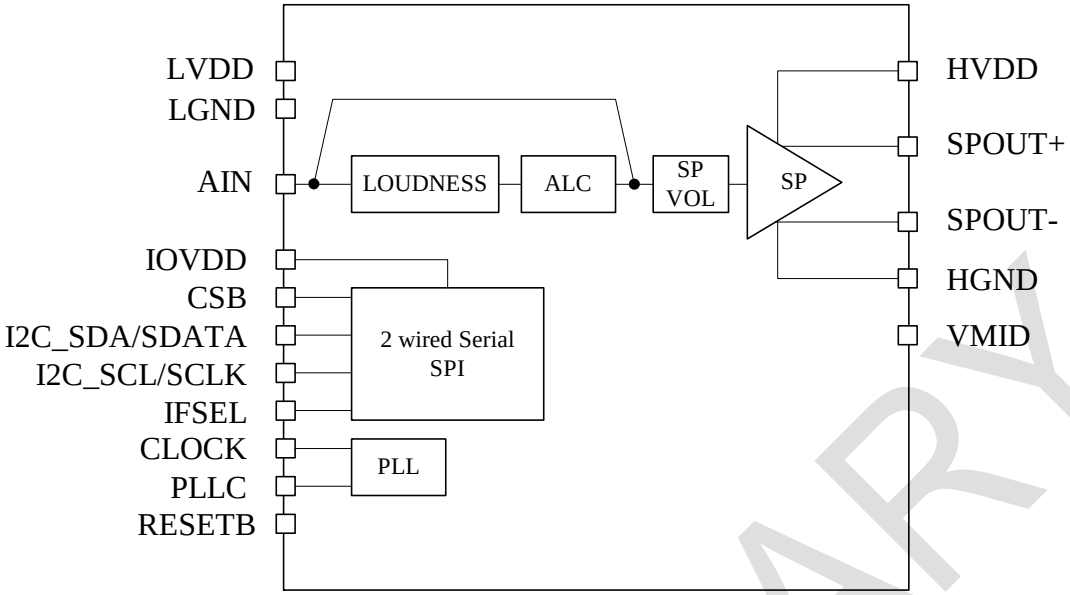
5) 8Ω 800mW Speaker amplifier

6) External System clock
- 32kHz~20MHz

7) Power supply voltage
- IOVDD : 1.65~3.60V
- LVDD : 2.25~2.75V (up to 2.95V under the special condition)
- HVDD: 2.7~5.5V

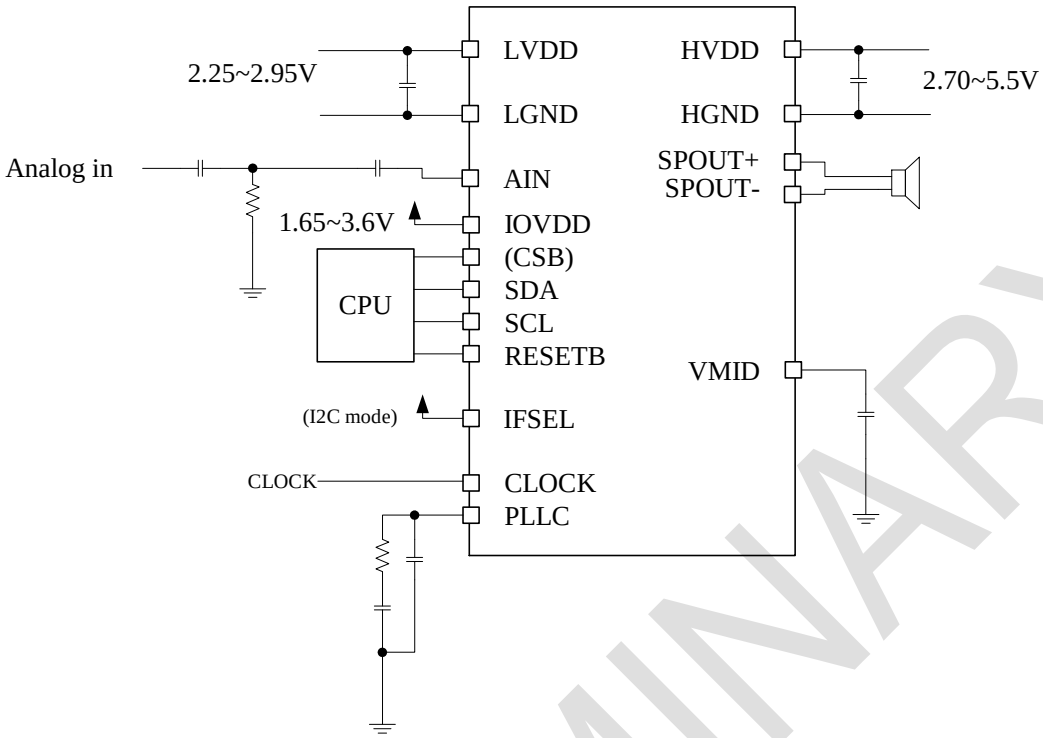
8) Packages
- 2.54mm * 2.42mm W-CSP
- 4mm * 4mm 20pin QFN (under development)

Block Diagram

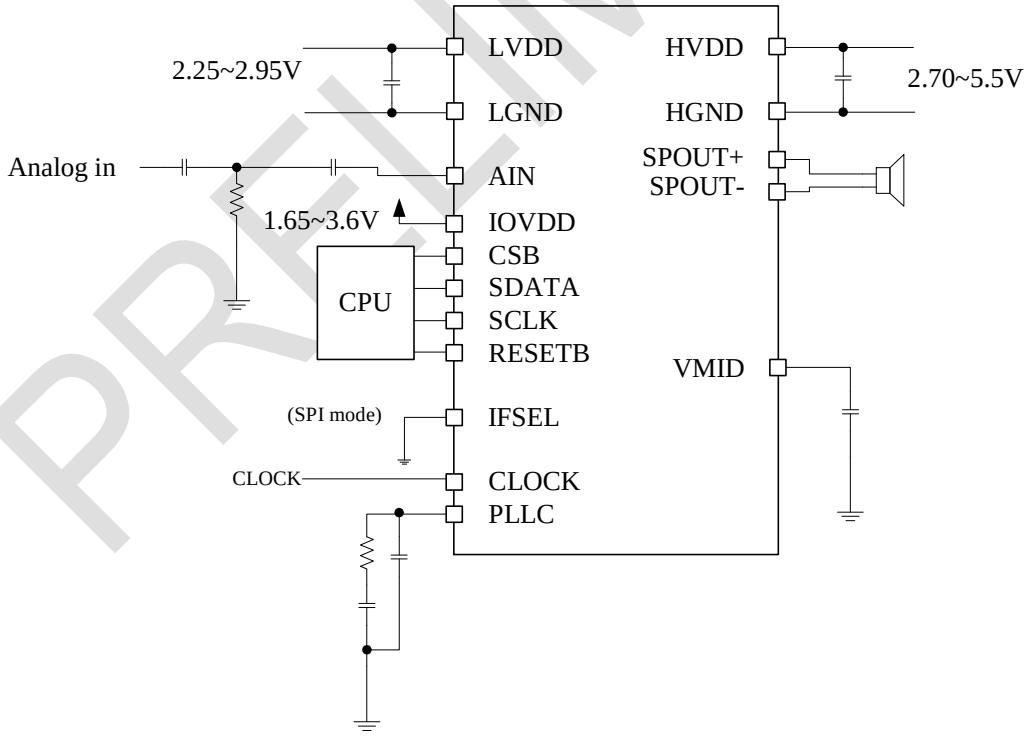


Application Example

ML2620
(2 wired serial inteface mode)



ML2620
(3 wired serial interface mode)



Pin Layout

W-CSP Package

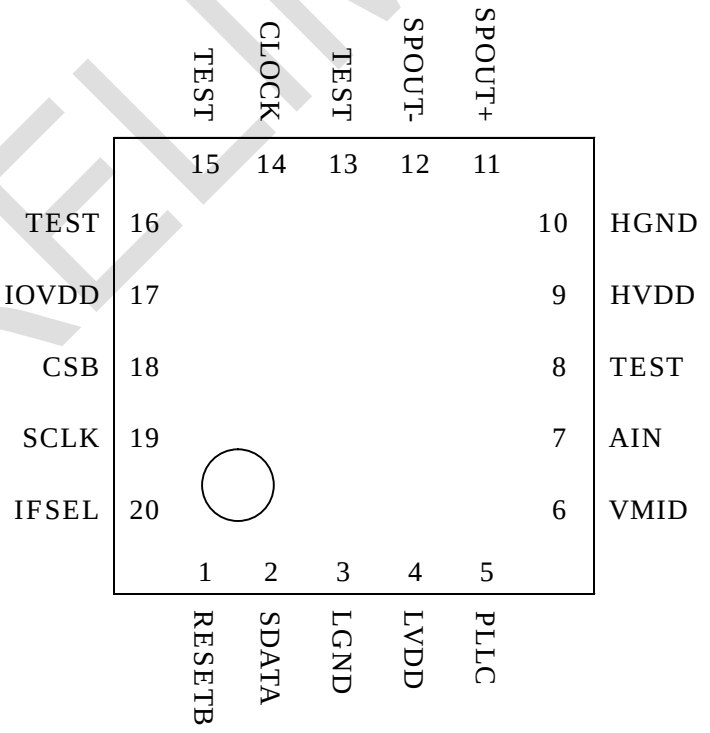
Bottom view

SDA/SDATA	SCL/SCLK	IOVDD	TEST	CLOCK	4
LGND	RESETB	CSB	TEST	TEST	3
PLLC	LVDD	IFSEL	SPOUT+	SPOUT-	2
TEST	VMID	AIN	HVDD	HGND	1
E	D	C	B	A	

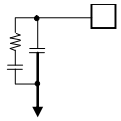
INDEX

QFN Package

Top View



Pin Description

`Pin no.		Pin name	IO	VDD	Explanation	Default status
1C	7	AIN	I	LVDD	Audio signal input pin	Hi-Z
2B	11	SPOUT+	O	HVDD	Speaker + output pin	HGND
2A	12	SPOUT-	O	HVDD	Speaker - output pin	HGND
4A	14	CLOCK	I	IOVDD	Master clock input pin	(input)
2E	5	PLLC	O	LVDD	The pin is to connect PLL loop back filter. Please connect resistor and capacitor like following figure.  PLLC pin	LGND
1D	6	VMID	O	LVDD	The pin is to connect capacitor for analog bias voltage. Please connect 1.0µF capacitor to LGND.	LGND
2C	20	IFSEL	I	IOVDD	CPU I/F select pin. When it is “L”, SPI interface is available. When “H”, 2-wired serial is available.	(input)
4E	2	SDA	I	IOVDD	data input pin of 2-wired serial interface	(input)
4D	19	SCL	I	IOVDD	clock input pin of 2 wired serial interface	(input)
3C	18	CSB	I	IOVDD	chip select pin of SPI	(input)
4E	2	SDATA	IO	IOVDD	serial data input / output pin of SPI	(input)
4D	19	SCLK	I	IOVDD		(input)
3D	1	RESETB	I	IOVDD	Reset and shutdown pin When “L”, the LSI is reset.	(input)
2D	4	LVDD	P	-	Power supply pin for low voltage part Please connect bypass capacitor to LGND	-
3E	3	LGND	P	-	GND pin for low voltage part	-
1B	9	HVDD	P	-	Power supply pin for high voltage part. Please connect bypass capacitor to HGND	-
1A	10	HGND	P	-		-
1E,3A, 3B,4B	8,13, 15,16	TEST	I		Test pin Please fix the pin as “L”.	-
4C	17	IOVDD	P	-	Power supply for IO. Please connect bypass capacitor to LGND.	-

Absolute Maximum Ratings

Items	Symbol	Condition	Rating	Unit
IOVDDSupply votage	IOVDD	-	-0.3~6.5	V
LVDDSupply votage	LVDD	-	-0.3~3.5	V
HVDDSupply votage	HVDD	-	-0.3~6.5	V
Input voltage	Vin	-	-0.3~VDD+0.3	V
Storage temperature	Tstg	-	-55~+125	°C
Power dissipation*1	Pd	Ta=25°C	910*1)	mW
Output current 1	IOSP	SPOUT+/- pin	-650~+650	mA
Output current 2	IOO	Except SPOUT+/-	-8 ~ +8	mA

Note) Do not short output pin to other output pin. (Output pin include output mode of IO pin.)
*1) Please refer to Recommended PCB Pattern Condition

Recommended Operating Condition

Item	Symbol	Condition	Rating	Unit
IOVDDSupply voltage	IOVDD	LVDD≦HVDD	1.65~3.60	V
LVDDSupply voltage	LVDD	LVDD≦HVDD	2.25~2.75	V
	LVDD	LVDD≦HVDD *1)	2.25~2.95	V
HVDDSupply voltage	HVDD	LVDD≦HVDD	2.7~5.5	V
Operating temperature	Top	-	-20~+85	°C

*1) Total operating time of the LSI must be less than 13000 hours.

Electrical Characteristics

DC Charactaristics

(IOVDD=1.65~3.60V,LVDD=2.25~2.95V, HVDD=2.7~5.5V, Ta=-20~+85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Applied pin
"H" Input voltage	VIH	LGND=0V	IOVDD*0.8	-	IOVDD	V	All Digital Input
"L" Input voltage	VIL	LGND=0V	0	-	IOVDD*0.2	V	All Digital Input
"H" Output voltage	VOH	IOH=-1mA	IOVDD*0.85	-	-	V	Except SDA pin
"L" Output voltage1	VOL1	IOL=1mA	-	-	IOVDD*0.25	V	Except SDA pin
"L" Output voltage2	VOL2	IOL=3mA, IOVDD>2V	-	-	0.4	V	SDA
"L" Output voltage3	VOL3	IOL=3mA, IOVDD<2V			IOVDD×0.2	V	SDA
"H" Input leakage current	IIH	VIH=IOVDD	-	-	10	µA	All Digital Input
"L" Input leakage current	IIL	VIL=LGND	-10	-	-	µA	All Digital Input
Operating current 1 LVDD	IDDO1L	Through mode no Load Sin1kHz-Full Scale output	-	-	8	mA	
Operating current 1 HVDD	IDDO1H		-	-	15	mA	
Operating current 2 LVDD	IDDO2L	Loudness mode no Load Sin1kHz-Full Scale input	-	-	22	mA	
Operating current 2 HVDD	IDDO2H		-	-	15	mA	
Standby current1	IDDS1	-20~25°C	-	1	5	µA	
Standby current 2	IDDS2	-20~50°C	-	-	20	µA	
Standby current 3	IDDS3	-20~85°C	-	-	90	µA	

Note) Please refer to next paragraph regarding typical cullent value.
Note) Standby current is total current of all power source surrent.

Current Consumption

The following table shows operating current typical value under each operating condition. This table is just for reference, it is not guaranteed.

(IOVDD=1.8V, LVDD=2.5V, HVDD=4.2V, Ta=25°C, no-load, no-signal, PLL off)

Operating Condition	Symbol	LVDD(mA)	HVDD(mA)	TOTAL(mW)
Speaker output without "LOUDNESS" effect (Clock stopped)	IDDO3	1.6	4.7	24

(IOVDD=1.8V, LVDD=2.5V, HVDD=4.2V, Ta=25°C, no-load, no-signal, PLL on)

Operating Condition	Symbol	LVDD(mA)	HVDD(mA)	TOTAL(mW)
Speaker output with "LOUDNESS" effect	IDDO4	14	4.7	55

The following table shows standby current typical value.

(IOVDD=1.8V, LVDD=2.5V, HVDD=4.2V)

Item	Symbol	Condition	Current value	Unit
Standby current 1	IDDST1	25°C	1	µA
Standby current 2	IDDST2	50°C	3	µA
Standby current 3	IDDST3	85°C	15	µA

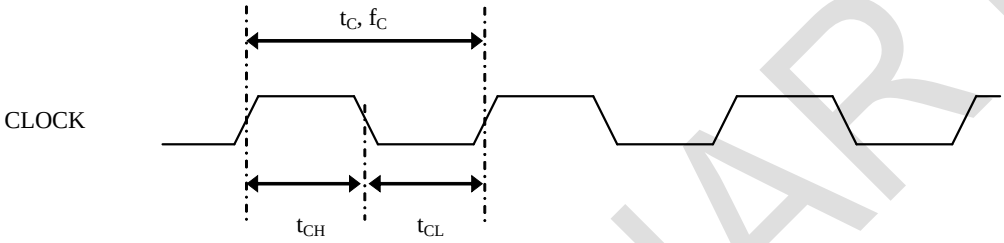
AC Charactaristics

Clock

PLL used (SAI Master)

(IOVDD=1.65~3.60V, LVDD=2.25~2.95V, HVDD=2.7~5.5V, Ta=-20~+85°C)

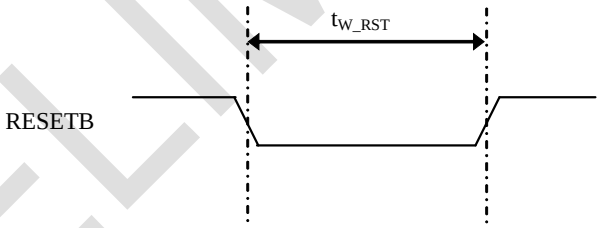
Item	Symbol	Min	Max.	Unit
CLOCK Frequency	f_C	32k	20M	Hz
CLOCK Period	t_C	$1/f_C$	$1/f_C$	ns
CLOCK "H" Length	t_{CH}	tC*0.4	-	ns
CLOCK "L" Length	t_{CL}	tC*0.4	-	ns



Reset

(IOVDD=1.65~3.60V, LVDD=2.25~2.95V, HVDD=2.7~5.5V, Ta=-20~+85°C)

Item	Symbol	Min	Max.	Unit
RESETB pulse width	t_{W_RST}	5	-	µs



2 wire serial interface

(IOVDD=1.65~3.60V, LVDD=2.25~2.95V, HVDD=2.7~5.5V, Ta=-20~+85°C, CL=30pF)

Item	Symbol	Standard mode		Fast mode		Unit
		Min	Max.	Min	Max.	
SCL Frequency	f_{SCL}	-	100	-	400	kHz
SCL "L" Length	t_{LOW}	4.7	-	1.3	-	µs
SCL "H" Length	t_{HIGH}	4.0	-	0.6	-	µs
Hold time under Repeat [Start] Condition	$t_{HD:STA}$	4.0	-	0.6	-	µs
Setup Time under Repeat[Start] Condition	$t_{SU:STA}$	4.0	-	0.6	-	µs
Data Hold Time	$t_{HD:DAT}$	0	3.45	0	0.9	µs
Data Setup Time	$t_{SU:DAT}$	250	-	100	-	ns
Setup Time under [Stop] Condition	$t_{SU:STO}$	4.0	-	0.6	-	µs

3 wire serial interface

(IOVDD=2.70~3.60V, LVDD=2.25~2.95V, HVDD=2.7~5.5V, Ta=-20~+85°C, CL=30pF)

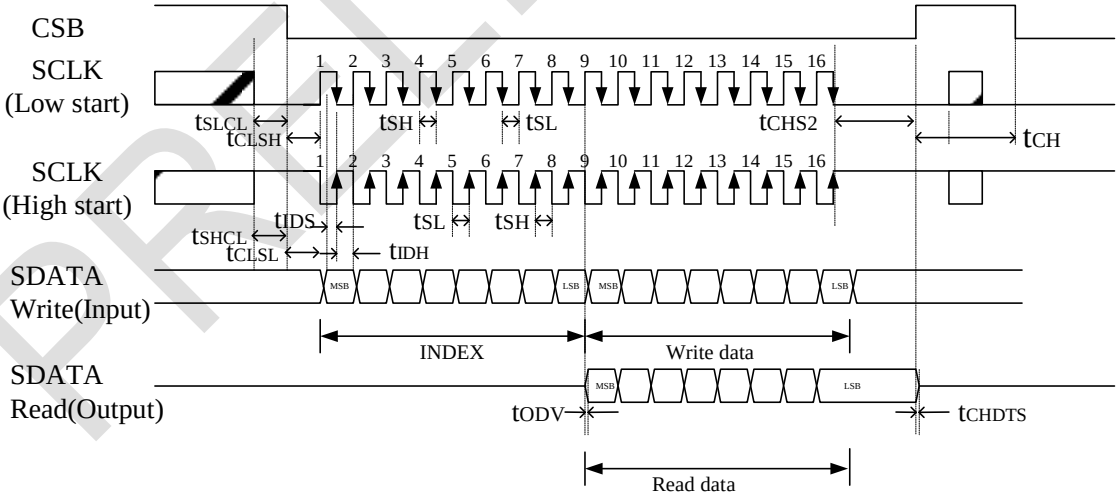
Item	Symbol	Min	Max.	Unit
SCLK Low to Chip Select enable	t_{SLCL}	100	-	ns
Chip Select enable to SCLK Low	t_{CLSL}	100	-	ns
Chip Select enable to SCLK High	t_{CLSH}	100	-	ns
SCLK High to Chip Select enable	t_{SHCL}	100	-	ns
SCLK High Pulse Width	t_{SH}	50	-	ns
SCLK Low Pulse Width	t_{SL}	50	-	ns
Input Data Hold time	t_{IDH}	30	-	ns
Input Data Setup time	t_{IDS}	30	-	ns
SCLK last edge to Chip Select disable	t_{CHS2}	100	-	ns
Chip Select High Pulse Width	t_{CH}	100	-	ns
Output Data Valid	t_{ODV}	-	40	ns
Chip Select High to Data Transition	t_{CHDTS}	-	40	ns

(IOVDD=1.65~2.70V, LVDD=2.25~2.95V, HVDD=2.7~5.5V, Ta=-20~+85°C, CL=30pF)

Item	Symbol	Min	Max.	Unit
SCLK Low to Chip Select enable	t_{SLCL}	100	-	ns
Chip Select enable to SCLK Low	t_{CLSL}	100	-	ns
Chip Select enable to SCLK High	t_{CLSH}	100	-	ns
SCLK High to Chip Select enable	t_{SHCL}	100	-	ns
SCLK High Pulse Width	t_{SH}	100	-	ns
SCLK Low Pulse Width	t_{SL}	100	-	ns
Input Data Hold time	t_{IDH}	30	-	ns
Input Data Setup time	t_{IDS}	30	-	ns
SCLK last edge to Chip Select disable	t_{CHS2}	100	-	ns
Chip Select High Pulse Width	t_{CH}	100	-	ns
Output Data Valid	t_{ODV}	-	80	ns
Chip Select High to Data Transition	t_{CHDTS}	-	80	ns

Two kinds of timing is supported depends on the SCLK pin level at data transfer start. Read or Write is selected by LSB logic of INDEX.

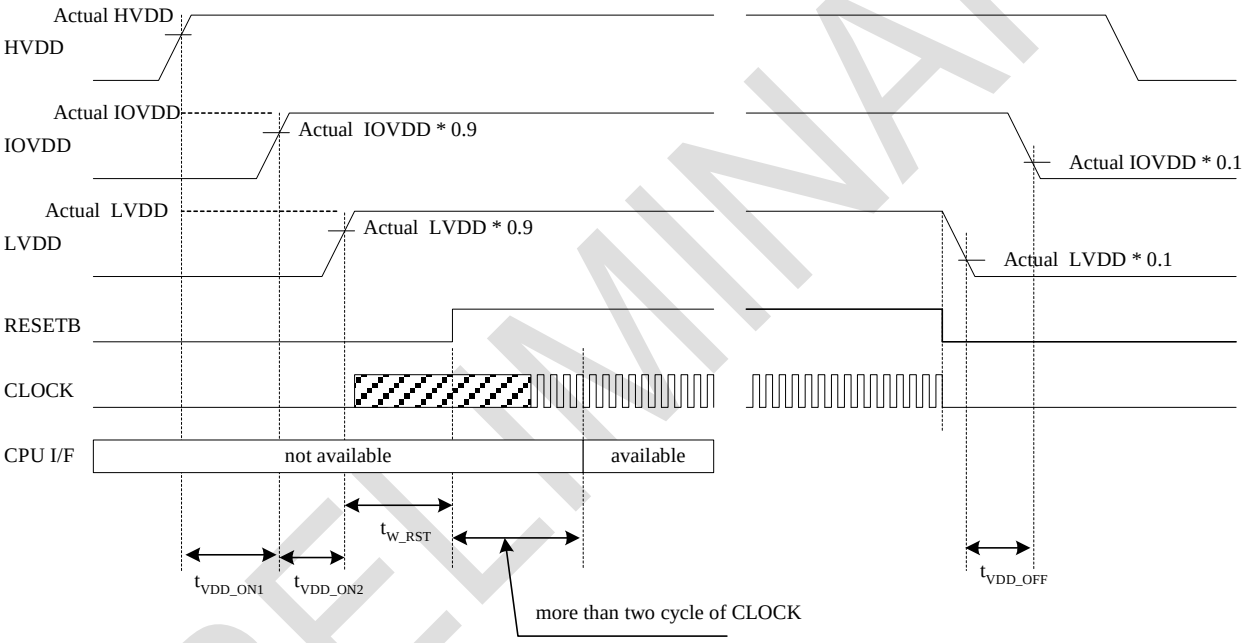
Characteristics of tODV, and tCHDTS differs to the condition of IOVDD.



Power Supply Sequence

Please power on/off the LSI with all kind of power at the same time. Each power supply should power up/down in 100ms. Also keep all power supply in the ON state or the OFF state. Please avoide partial ON or partial OFF status.

Item	Symbol	Min	Typ	Max	Unit
Power On Delay Time 1	t_{VDD_ON1}	0	-	-	Ms
Power On Delay Time 2	t_{VDD_ON2}	0	-	100	Ms
Power Off Delay Time	t_{VDD_OFF}	0	-	100	Ms
Reset Time after Power On	t_{W_RST}	5	-	-	μs



Analog Characteristics

(IOVDD=1.65~3.60V, LVDD=2.25~2.95V, HVDD=2.7~5.5V, Ta=-20~+85°C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Input Resistance *1)	R_{LIN}	LINVL = 0dB	30	44.2	60	kΩ
		LINVL = -12dB	50	70.7	90	kΩ
Output Resistance *2)	R_{LOAD}		-	8	-	Ω

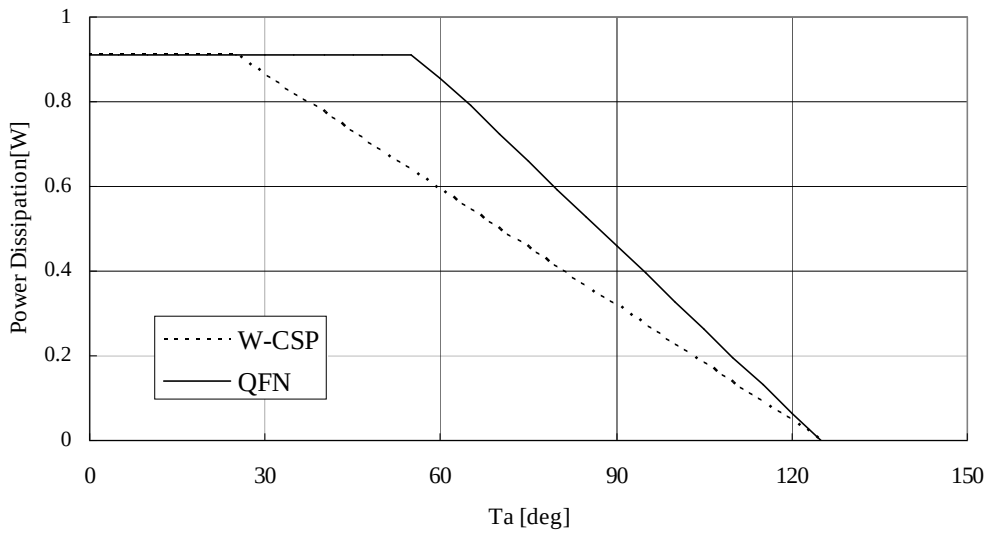
*1) Apply for AIN
*2) Apply for SPOUT+ / SPOUT-

Power Derating Curves

(Condition: JEDEC 2 layers)

Item	Package	Thermal resistance	Unit
θja	W-CSP	110.0	°C /W
ψjt		0.02	°C /W
θjc		0.24	°C /W
θja	QFN	76.0(T.B.D.)	°C /W
ψjt		0.40(T.B.D.)	°C /W
θjc		9.42(T.B.D.)	°C /W

Power Derating Curves



Revision history

Date	Page	Notes	Revision
07/08/27	All	Preliminary version 1 release	1
07/08/31	8	Specified uncertain TBD in Absolute maximum rating.	2
07/08/31	15	Add Thermal resistor characteristics.	2

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