FEDL9842FULL-02

OKI Semiconductor

This version: Apr. 2001
Previous version: May 1998

MSM9842

Playback LSI with Built-in FIFO

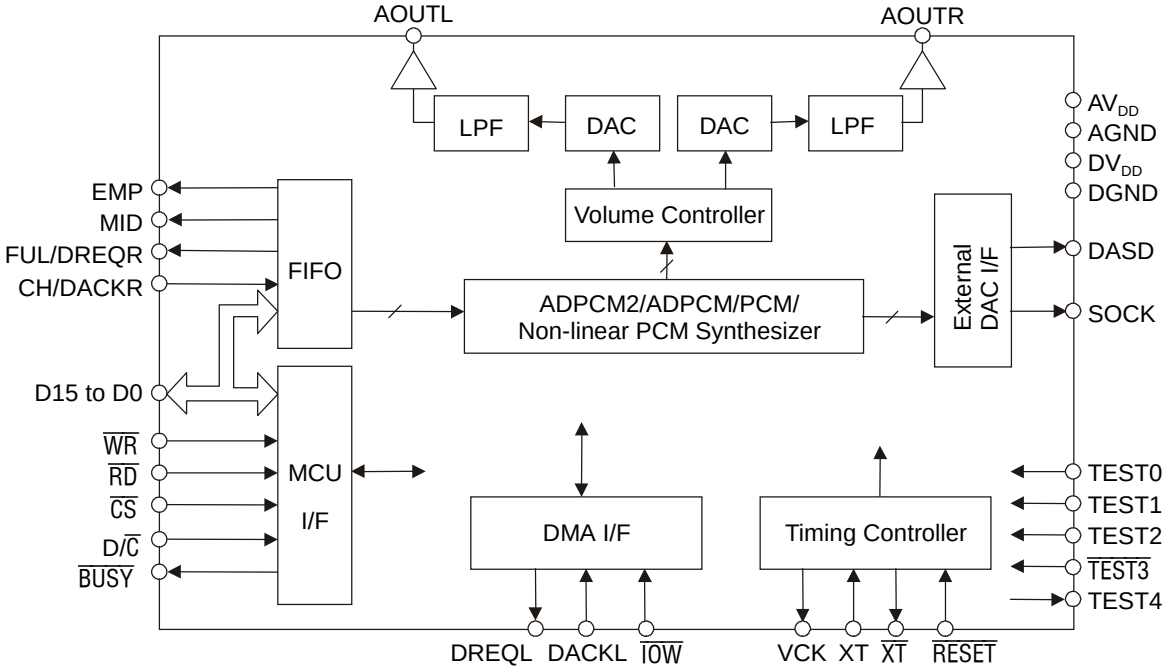
GENERAL DESCRIPTION

The MSM9842 is a mono/stereo playback LSI with a built-in 1K bit FIFO for easy interface with external systems or non-semiconductor memory. It utilizes multiple playback modes, including the new OKI ADPCM2 algorithm, which allows for even higher quality sound reproduction. The playback function of the MSM9842 is controlled by a CPU via 8/16-bit bus interface.

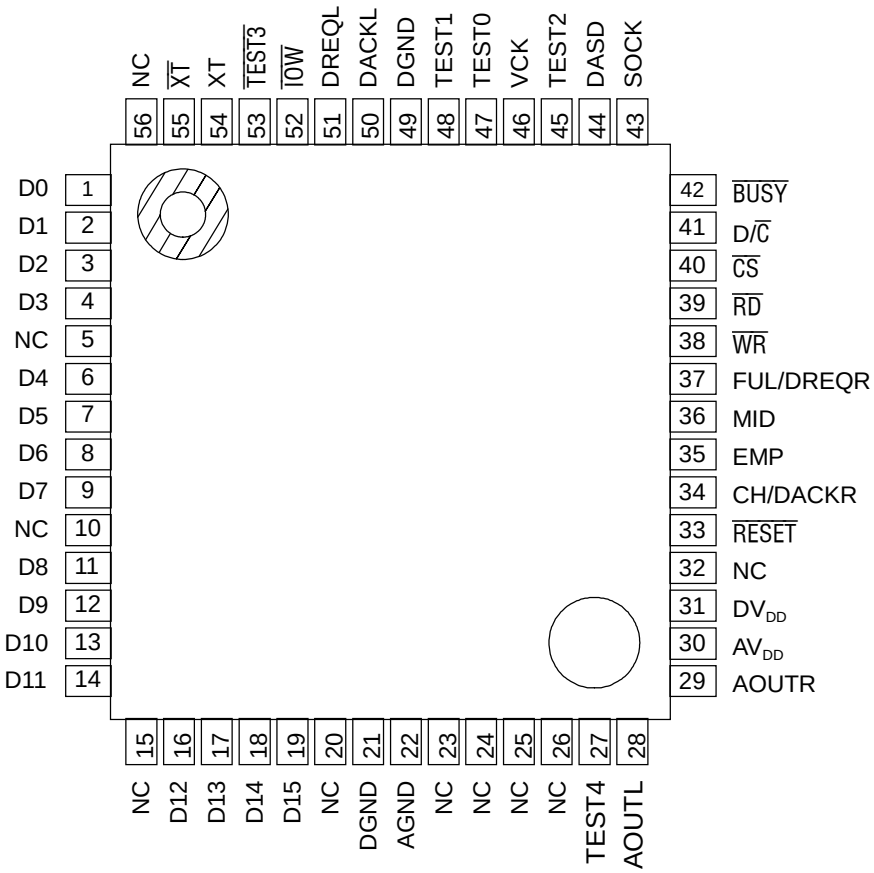
FEATURES

- 16/8-bit bus interface support
- FIFO capacity: 1024 bits
  (buffering time of 32 ms when using 8 kHz sampling frequency, 4-bit ADPCM2/ADPCM, and in monaural playback)
- Supports four compression algorithms for playback:
  4, 5, 6, 7, 8-bit ADPCM2; 4-bit ADPCM; 8, 16-bit PCM; and 8-bit OKI Nonlinear PCM
- Sampling frequency: 4.0 kHz, 6.4 kHz, 8.0 kHz, 12.8 kHz, 16.0 kHz, 32.0 kHz (f_{OSC} = 4.096 MHz)
- Sampling frequency: 22.05 kHz, 44.1 kHz (f_{OSC} = 5.6448 MHz)
- DMA interface support
- Volume control (8 steps: 0 to –21 dB, 3 dB step)
- Built-in 14-bit D/A converter
- Built-in low pass filter (LPF) : digital filter
- Power supply voltage: 2.7 to 5.5 V
- Package:
  56-pin plastic QFP (QFP56-P-910-0.65-2K) (Product name: MSM9842GA)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC : No Connection

56-pin plastic QFP

PIN DESCRIPTIONS (1/2)

Pin No.	Symbol	Type	Description
11-14, 12-19	D15-D8	I/O	For 8-bit bus interface, the command allows these pins to be configured to be inputs to input data to and from an external memory. Otherwise, these pins are configured to be inputs only. For 16-bit interface, these pins are a bidirectional data bus to input data to and from an external microcontroller and memory.
1-4, 6-9	D7-D0	I/O	Bidirectional data bus to input data and output status to and from an external microcontroller and memory.
38	$\overline{WR}$	I	Write pulse input pin. This pin pulses “L” when command or voice data is input to D15-D0 pins.
39	$\overline{RD}$	I	Read pulse input pin. This pin pulses “L” when status is output to D15-D0 pins.
40	$\overline{CS}$	I	Accepts write pulse and read pulse when this pin is “L”. Does not accept write pulse and read pulse when this pin is “H”.
41	D/$\overline{C}$	I	Voice data is input to D15-D0 pins when this pin is “H”. Command is input to and status is output from D7-D0 pins when this pin is "L".
42	$\overline{BUSY}$	O	This pin outputs a "L" level during PLAYBACK or PAUSE.
35	EMP	O	“H” level indicates that there is no data in FIFO memory. Active “H” can be changed to active “L” by command input.
36	MID	O	“H” level indicates that more than half of the FIFO memory space is filled with data. Voice synthesis starts when MID changes to “H” level. Active “H” can be changed to active “L” by command input. This pin outputs a synchronizing signal for voice data input and output when non-use of FIFO is selected.
37	FUL/DREQR	O	“H” level indicates that FIFO memory is full of data. This pin is “H” and data cannot be written in FIFO memory. Active “H” can be changed to active “L” by command input. When DMA transfer and stereo playback are selected, “H” level DREQR outputs a signal to request a DMA transfer of right voice data. Active “H” can be changed to active “L” by command input.
34	CH/DACKR	I	When stereo playback is selected and CH is “H”, voice data is written in right FIFO memory, and the EMP, MID or FUL pin outputs the status of right FIFO memory. When CH is “L”, data is written in right FIFO memory, and the EMP, MID or FUL pin outputs the status of left FIFO memory. Set this pin to “L” during monophonic playback. When DMA transfer and stereo playback are selected, DACKR is selected. In this case, DACKR outputs a DMA transfer acknowledge signal of right voice data. When DACKR is “L”, the $\overline{IOW}$ signal is accepted. Active “L” can be changed to active “H” by command input.
51	DREQL	O	When DMA transfer is selected by command input, “H” level DREQL outputs a signal to request a DMA transfer of voice data to the DMA controller. When stereo playback is selected, “H” level DREQL outputs a signal to request a DMA transfer of left voice data to the DMA controller. Active “H” can be changed to active “L” by command input.

PIN DESCRIPTIONS (2/2)

Pin No.	Symbol	Type	Description
50	DACKL	I	DACKL inputs a signal when DMA transfer is permitted by the DMA controller. When DACKL is "L", $\overline{IOW}$ signal is accepted. When stereo playback is selected, DACKL is a DMA transfer acknowledge signal of left voice data from the DMA controller. Active "L" can be changed to active "H" by command input. If DMA transfer is not used, set this pin to "H" level.
52	$\overline{IOW}$	I	Signal to write external memory data to MSM9842 during DMA transfer. If DMA transfer is not used, set this pin to "H" level.
44	DASD	O	16-bit serial data output pin when external DAC is used.
43	SOCK	O	Synchronizing clock for 16-bit serial data output when external DAC is used.
54 55	XT $\overline{XT}$	I O	Oscillator connection pins. When external clock is used, input clock into XT pin and leave $\overline{XT}$ pin open.
46	VCK	O	Outputs sampling frequency selected at playback. This sampling frequency is used as a synchronizing signal when external DAC is used.
33	$\overline{RESET}$	I	When this pin is "L", the LSI is initialized.
47 48 45	TEST0 TEST1 TEST2	I	Pins for testing. Set the pins to "L".
53	$\overline{TEST3}$	I	Pin for testing. Set the pin to "H".
27	TEST4	O	Output pin for testing. Set the pin to "OPEN".
28	AOUTL	O	Left side output pin for built-in LPF. This is the output pin of playback waveforms, and is connected to the amplifier for driving speakers.
29	AOUTR	O	Right side output pin for built-in LPF. This is the output pin of playback waveforms, and is connected to the amplifier for driving speakers.
31	DV_{DD}	—	Digital power supply pin. Insert a minimum 0.1 μF bypass capacitor between this pin and DGND pin.
21,49	DGND	—	Digital GND pin.
30	AV_{DD}	—	Analog power supply pin. Insert a minimum 0.1 μF bypass capacitor between this pin and AGND pin.
22	AGND	—	Analog GND pin.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +7.0	V
Input Voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Power Supply Voltage	V_{DD}	DGND = AGND = 0 V	2.7 to 5.5	V
Operating Temperature	T_{OP}	—	–40 to +85	°C
Master Clock Frequency	f_{OSC}	—	4.0 to 6.0	MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics (5V)

DV_{DD} = AV_{DD} = 4.5 to 5.5 V, DGND = AGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High-level Input Voltage	V_{IH}	—	$V_{DD} \times 0.85$	—	—	V
Low-level Input Voltage	V_{IL}	—	—	—	$V_{DD} \times 0.2$	V
High-level Output Voltage	V_{OH}	I_{OH} = –40 µA	V_{DD} –0.3	—	—	V
Low-level Output Voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.45	V
High-level Input Current (*1)	I_{IH1}	$V_{IH} = V_{DD}$	—	—	10	µA
High-level Input Current (*2)	I_{IH2}	$V_{IH} = V_{DD}$	—	—	20	µA
High-level Input Current (*3)	I_{IH3}	$V_{IH} = V_{DD}$	30	150	300	µA
Low-level Input Current (*1)	I_{IL1}	V_{IL} = GND	–10	—	—	µA
Low-level Input Current (*2)	I_{IL2}	V_{IL} = GND	–20	—	—	µA
Operating Current Consumption	I_{DD}	f_{osc} = 4.096 MHz, without load	—	15	30	mA
Standby Current Consumption	I_{DDS}	At power-down, without load Ta = –40 to +70°C	—	—	10	µA
		At power-down, without load Ta = –40 to +85°C	—	—	50	µA

*1 Applicable to input excluding XT pin.
*2 Applicable to XT pin.
*3 Applicable to TEST0, TEST1.

DC Characteristics (3V)

DV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High-level Input Voltage	V_{IH}	—	$V_{DD} \times 0.85$	—	—	V
Low-level Input Voltage	V_{IL}	—	—	—	$V_{DD} \times 0.2$	V
High-level Output Voltage	V_{OH}	I_{OH} = –40 µA	V_{DD} –0.3	—	—	V
Low-level Output Voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.45	V
High-level Input Current (*1)	I_{IH1}	$V_{IH} = V_{DD}$	—	—	10	µA
High-level Input Current (*2)	I_{IH2}	$V_{IH} = V_{DD}$	—	—	20	µA
High-level Input Current (*3)	I_{IH3}	$V_{IH} = V_{DD}$	10	50	100	µA
Low-level Input Current (*1)	I_{IL1}	V_{IL} = GND	–10	—	—	µA
Low-level Input Current (*2)	I_{IL2}	V_{IL} = GND	–20	—	—	µA
Operating Current Consumption	I_{DD}	f_{osc} = 4.096 MHz, without load	—	10	20	mA
Standby Current Consumption	I_{DDS}	At power-down, without load Ta = –40 to +70°C	—	—	10	µA
		At power-down, without load Ta = –40 to +85°C	—	—	50	µA

*1 Applicable to input excluding XT pin.
*2 Applicable to XT pin.
*3 Applicable to TEST0, TEST1.

Analog Characteristics (5V)

DV_{DD} = AV_{DD} = 4.5 to 5.5 V, DGND = AGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
D/A Output Relative Error	$\|V_{DAE}\|$	No load	—	—	10	mV
AOUTL Output Load Resistance	R_{AOUT}	—	50	—	—	kΩ
DAC Output Impedance	R_{DAO}	When DAC output is selected	15	25	35	kΩ
AOUTL, AOUTR output impedance during standby mode	R_{SAO}	During standby mode or power-down mode	15	25	35	kΩ

Analog Characteristics (3V)

DV_{DD} = AV_{DD} = 2.7 to 3.6 V, DGND = AGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
D/A Output Relative Error	$\|V_{DAE}\|$	No load	—	—	5	mV
AOUTL Output Load Resistance	R_{AOUT}	—	50	—	—	kΩ
DAC Output Impedance	R_{DAO}	When DAC output is selected	15	25	35	kΩ
AOUTL, AOUTR output impedance during standby mode	R_{SAO}	During standby mode or power-down mode	15	25	35	kΩ

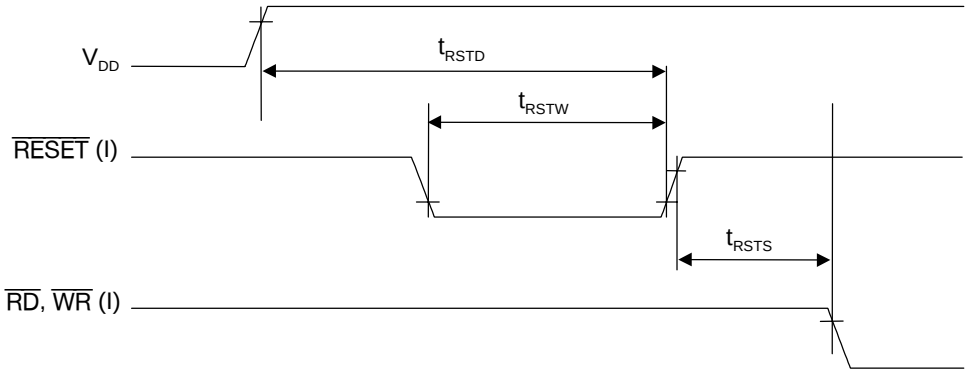
AC Characteristics

DV_{DD} = AV_{DD} = 2.7 to 5.5 V, DGND = AGND = 0 V, Ta = –40 to +85°C

Parameter	Symbol	Min.	Typ.	Max.	Unit
$\overline{RESET}$ Pulse Width	t_{RSTW}	300	—	—	ns
Setup Time after Rise of Power Supply for Fall of $\overline{RESET}$	t_{RSTD}	500	—	—	ns
Time to Active First $\overline{RD}$, $\overline{WR}$ after Fall of $\overline{RESET}$	t_{RSTS}	200	—	—	ns
$\overline{RD}$ Pulse Width	t_{RR}	160	—	—	ns
$\overline{CS}$, D/$\overline{C}$, CH Setup and Hold Time for $\overline{RD}$	t_{CR}	30	—	—	ns
Time from Fall of $\overline{RD}$ till Status Data Definition	t_{DRE}	—	—	120	ns
Time from Fall of $\overline{RD}$ till Status Data Float	t_{DRF}	—	10	50	ns
Time from Rise of $\overline{RD}$ till Fall of Next $\overline{RD}$ during Status Read	t_{CRC}	500	—	—	ns
$\overline{WR}$ Pulse Width	t_{WW}	160	—	—	ns
$\overline{CS}$, D/$\overline{C}$, CH Setup and Hold Time for $\overline{WR}$	t_{CW}	30	—	—	ns
Setup Time of Data and Command for Rise of $\overline{WR}$	t_{DWS}	100	—	—	ns
Setup Time of Playback Start Command for Rise of $\overline{WR}$	t_{DWS}	t_{ww} + 50	—	—	ns
Hold Time of Data and Command for Rise of $\overline{WR}$	t_{DWH}	10	—	—	ns
Time from Rise of $\overline{WR}$ till Fall of Next $\overline{WR}$ (1) during Command Write	t_{CWC}	500	—	—	ns
Time from Rise of $\overline{WR}$ till Fall of Next $\overline{WR}$ (2) during Data Write	t_{CWC}	200	—	—	ns
Time from Rise of MID till Rise of $\overline{WR}$ (For synchro timing when FIFO memory is not used)	t_{MW}	2	—	15	µs
MID pulse width (For synchro timing when FIFO memory is not used)	t_{MM}	15.6	—	125	µs
$\overline{IOW}$ Pulse Width	t_{IOWW}	160	—	—	ns
Setup and Hold Time of DACKL/R for $\overline{IOW}$	t_{DW}	10	—	—	ns
Setup Time of Data for Rise of $\overline{IOW}$	t_{IOWE}	100	—	—	ns
Hold Time of Data for Rise of $\overline{IOW}$	t_{IOWF}	10	—	—	ns
Time from Rise of $\overline{IOW}$ till Fall of Next $\overline{IOW}$	t_{IOWC}	200	—	—	ns

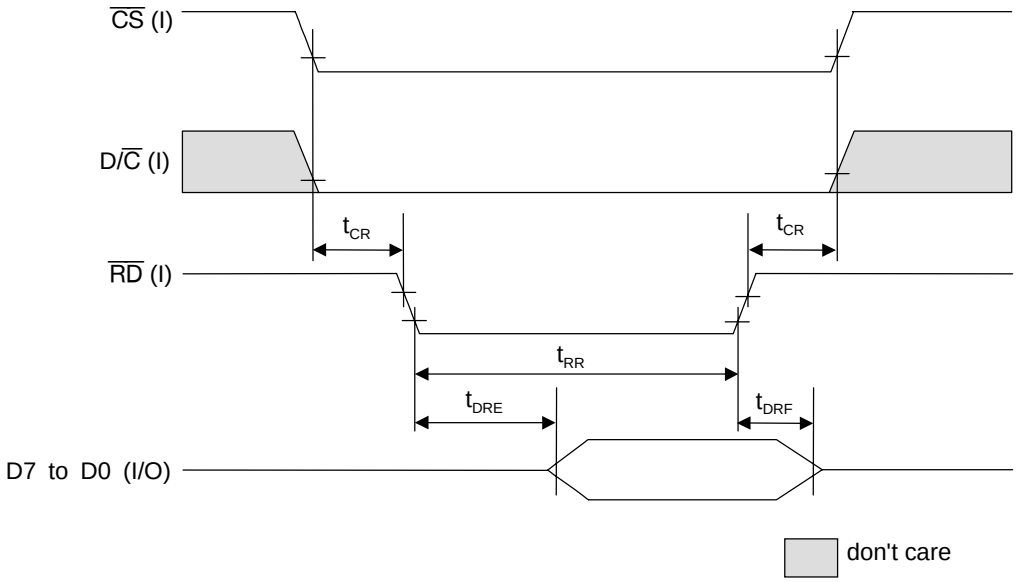
TIMING DIAGRAMS

Reset Timing

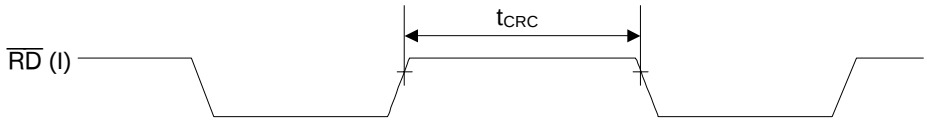


Read Timing

1. Status Read Timing

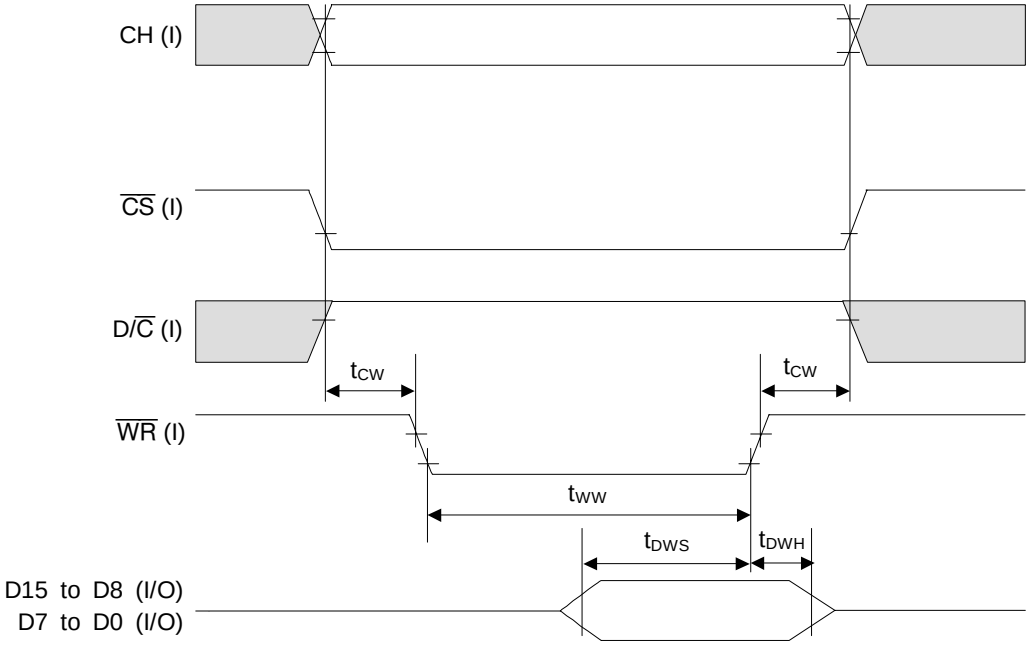


2. Read Cycle Timing

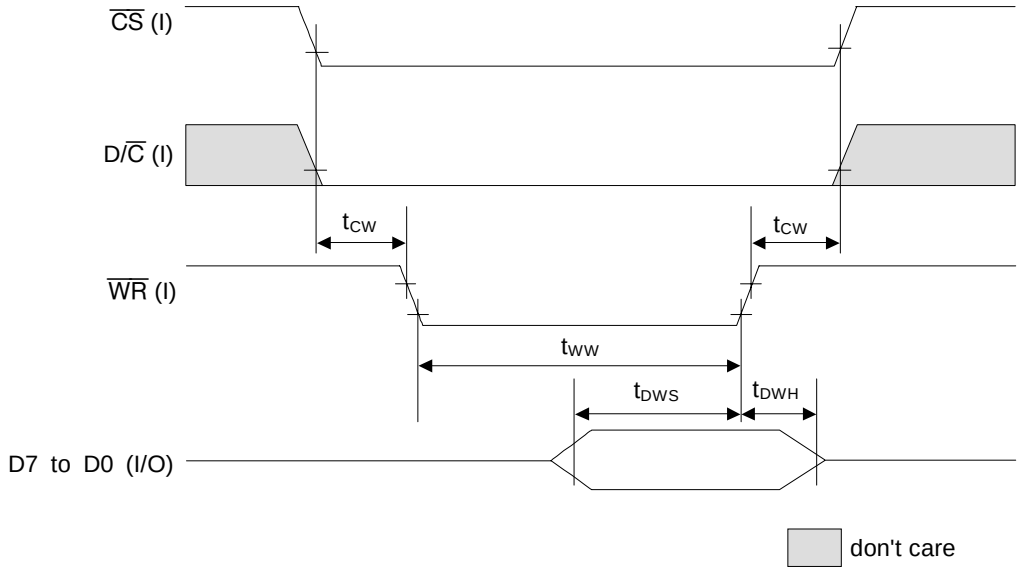


Write Timing

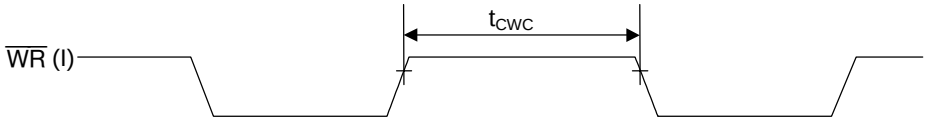
1. Data Write Timing



2. Command Write Timing

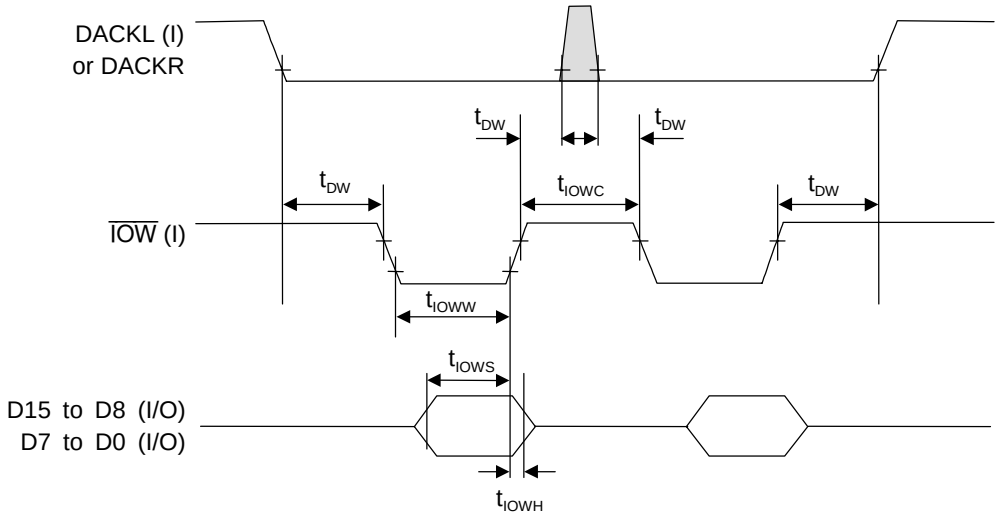


3. Write Cycle Timing

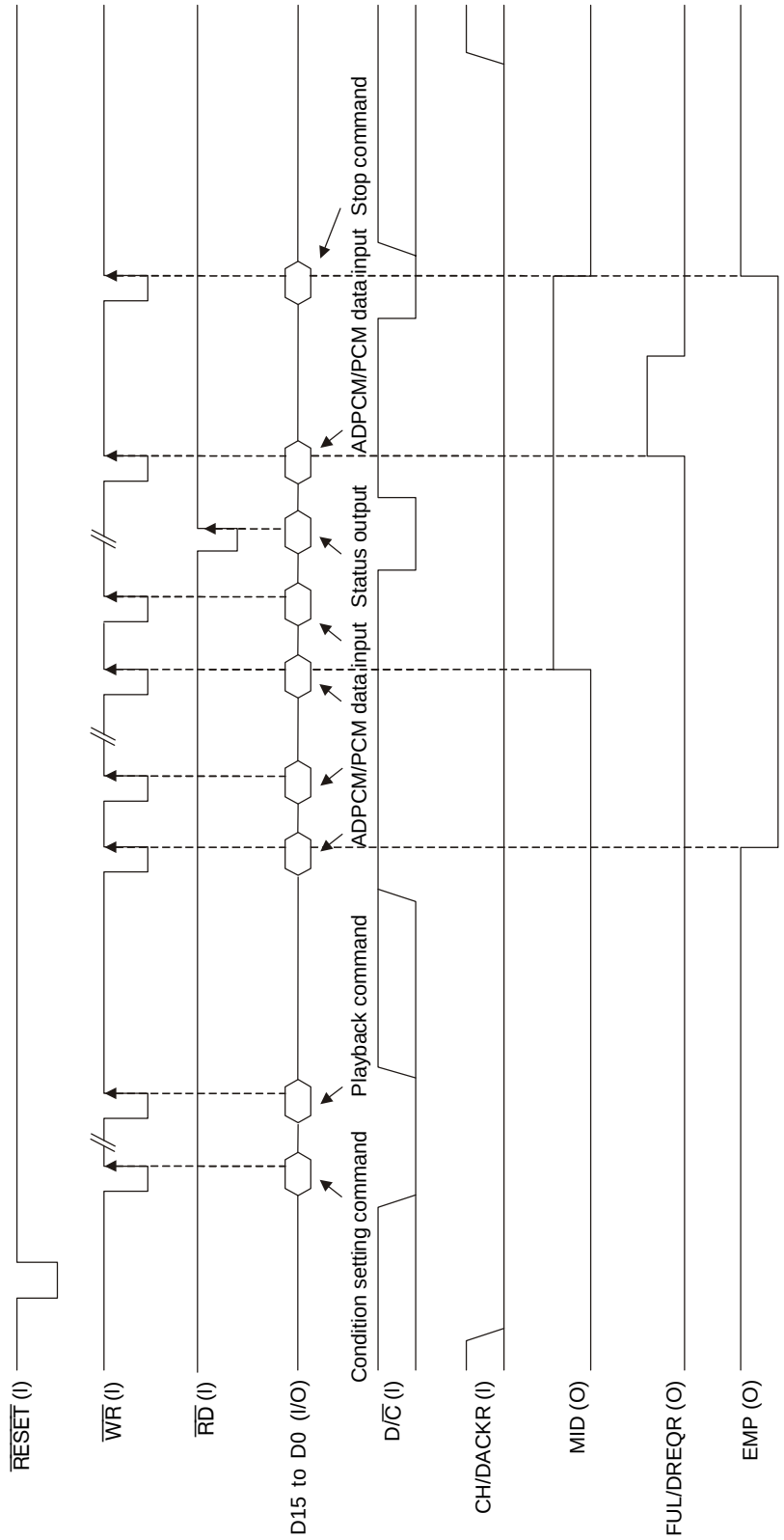


DMA Transfer Timing

1. $\overline{IOW}$ (during 2-byte writing)

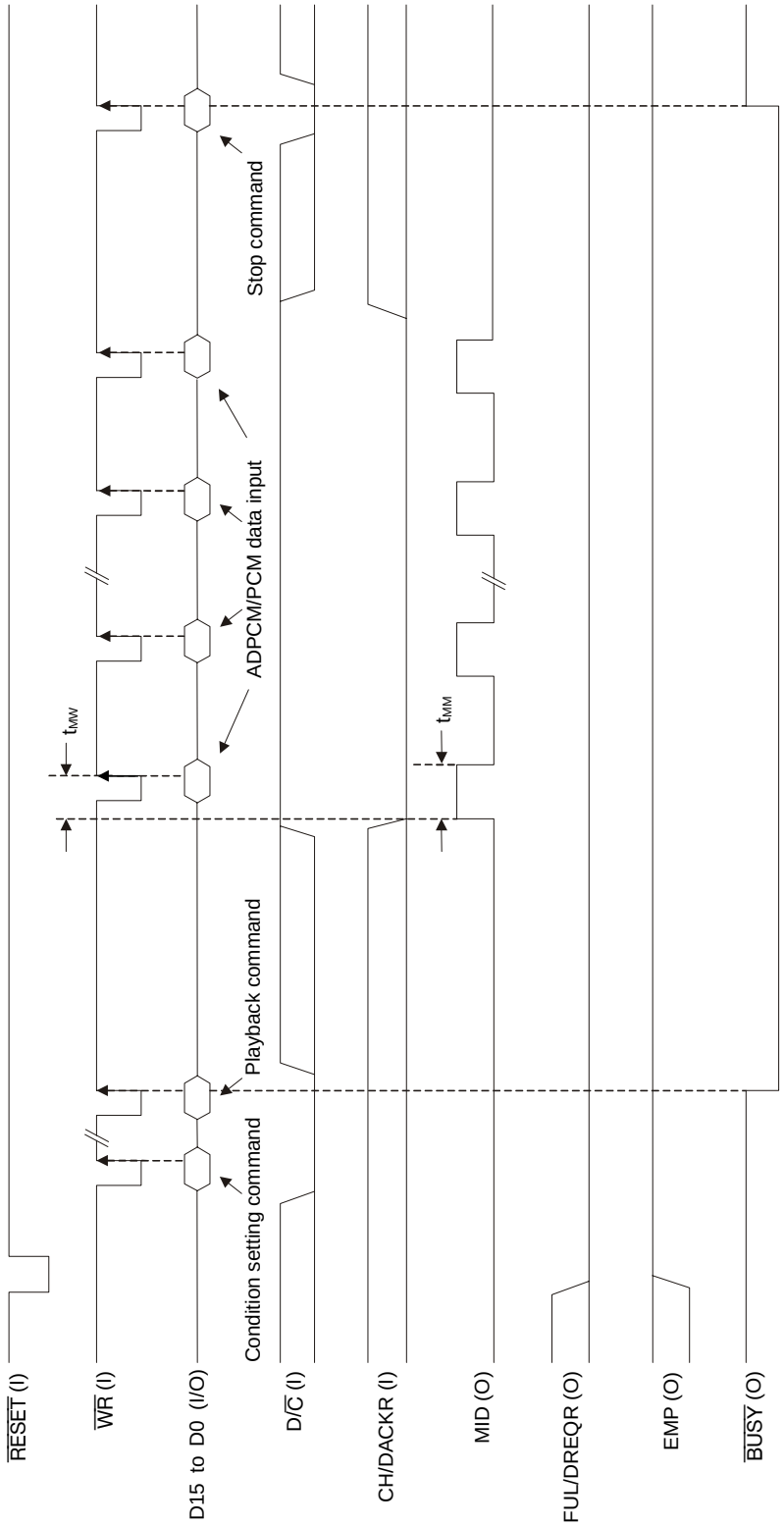


Monophonic Playback Timing (When FIFO memory is used)



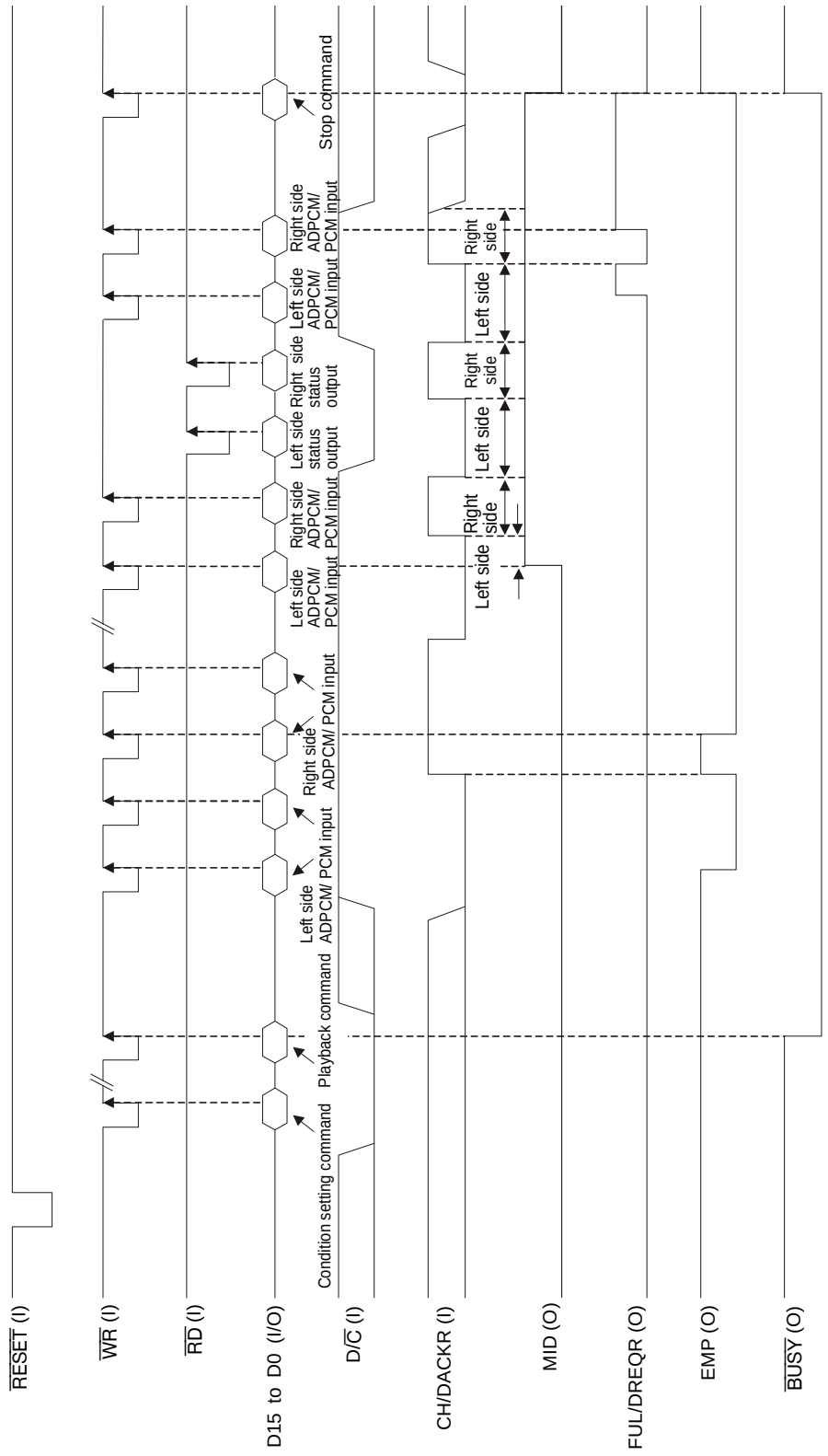
Note) Enter a condition setting command for every item to be set.

Monophonic Playback Timing (When FIFO memory is not used)



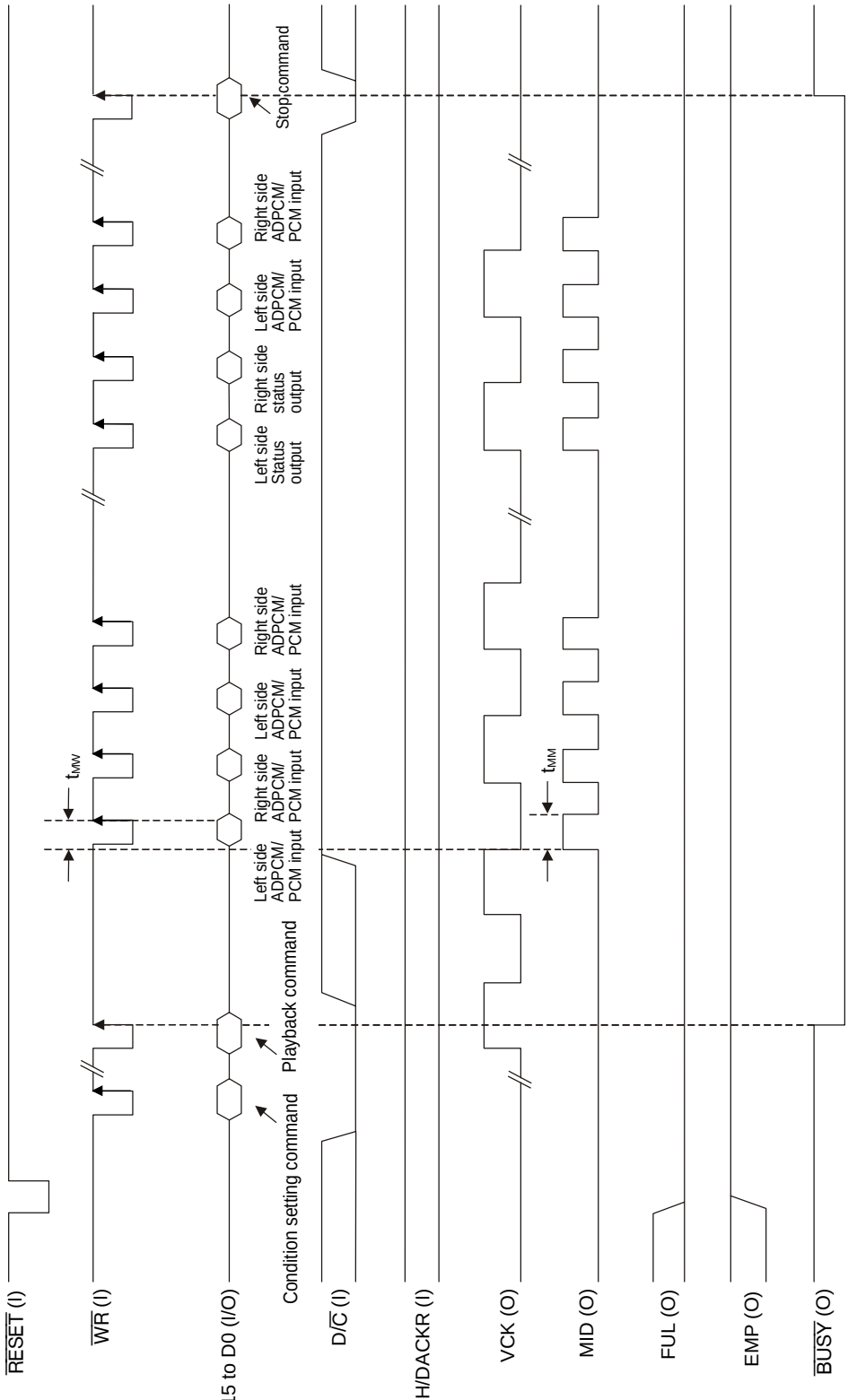
Note) Enter a condition setting command for every item to be set.

Stereophonic Playback Timing (When FIFO memory is used)



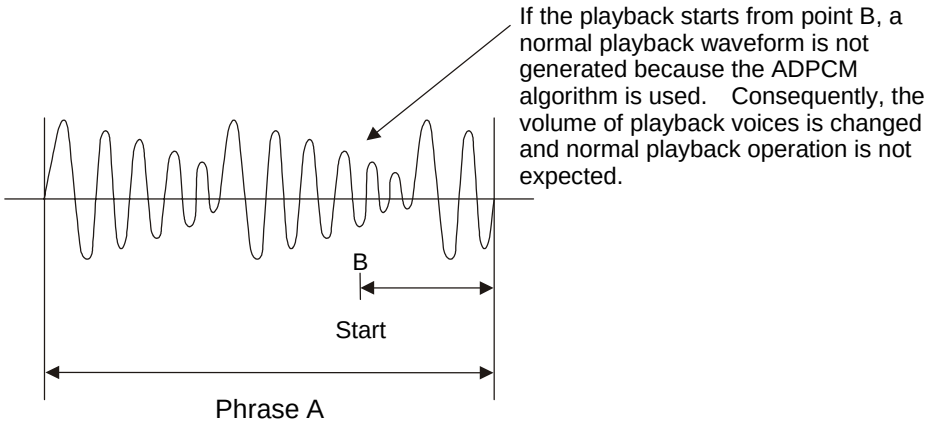
Note) Enter a condition setting command for every item to be set.

Stereophonic Playback Timing (When FIFO memory is not used)



Note) Enter a condition setting command for every item to be set.

Note : Starting the playback in the midst of a phrase causes the MSM9842 to generate an abnormal playback waveform because the ADPCM algorithm is used. Consequently, a normal playback operation is not made.



FUNCTIONAL DESCRIPTION

Voice synthesis method

The MSM9842 supports four PCM methods to process various kinds of voices :4-bit ADPCM; 4-, 5-, 6-, 7-, or 8-bit ADPCM2; 8- or 16-bit straight PCM; and 8-bit non-linear PCM methods.

1. 4-bit ADPCM method (Adaptive Differential Pulse Code Modulation)
   This method encodes 4-bit data while adaptively varying the basic quantization width "Δ" at each sampling. This method very effectively processes human and animal voices and natural sounds, reducing voice data storage space.

2. 4-, 5-, 6-, 7-, or 8-bit ADPCM2 method
   This method has higher sound reproduction quality than the ADPCM method. The ADPCM2 method offers five compression methods (4-, 5-, 6-, 7-, or 8-bit). Note that data used in the 4-bit ADPCM method is not compatible with data in the 4-bit ADPCM2 method.
   Data conversion for these methods can be made by a development tool.

3. 8- or 16-bit straight PCM method
   This method has the highest sound reproduction characteristics in all frequencies (of the above four PCM methods). This method is suitable for sound effects having high frequencies and sounds having pulse-like waveforms.

4. 8-bit non-linear PCM method
   The method emphasizes the value of each sound wave in the range from 7/16 V_{DD} to 9/16 V_{DD} and processes it with 10-bit straight PCM tone quality. It is effective in improving the tone quality of frequency low voices and sounds.

Data configuration when 8-bit bus is used

"X" is "don't care" during playback.

1. 4-bit ADPCM method and 4-bit ADPCM2 method

D7	D6	D5	D4	D3	D2	D1	D0
MSB1	3SB1	2SB1	LSB1	MSB2	3SB2	2SB2	LSB2

2. 5-bit ADPCM2 method

D7	D6	D5	D4	D3	D2	D1	D0
×	×	×	MSB1	4SB1	3SB1	2SB1	LSB1

3. 6-bit ADPCM2 method

D7	D6	D5	D4	D3	D2	D1	D0
×	×	MSB1	5SB1	4SB1	3SB1	2SB1	LSB1

4. 7-bit ADPCM2 method

D7	D6	D5	D4	D3	D2	D1	D0
×	MSB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1

5. 8-bit ADPCM2 method, 8-bit straight PCM method, and 8-bit non-linear PCM method

D7	D6	D5	D4	D3	D2	D1	D0
MSB1	7SB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1

6. 16-bit straight PCM method

D7	D6	D5	D4	D3	D2	D1	D0	
MSB1	15SB1	14SB1	13SB1	12SB1	11SB1	10SB1	9SB1	1st transfer
8SB1	7SB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1	2nd transfer

Data configuration when 16-bit bus is used

"X" is "don't care" during playback.

1. 4-bit ADPCM method and 4-bit ADPCM2 method

D15	D14	D13	D12	D11	D10	D9	D8
MSB1	3SB1	2SB1	LSB1	MSB2	3SB2	2SB2	LSB2
D7	D6	D5	D4	D3	D2	D1	D0
MSB3	3SB3	2SB3	LSB3	MSB4	3SB4	2SB4	LSB4

2. 5-bit ADPCM2 method

D15	D14	D13	D12	D11	D10	D9	D8
×	×	×	MSB1	4SB1	3SB1	2SB1	LSB1
D7	D6	D5	D4	D3	D2	D1	D0
×	×	×	MSB2	4SB2	3SB2	2SB2	LSB2

3. 6-bit ADPCM2 method

D15	D14	D13	D12	D11	D10	D9	D8
×	×	MSB1	5SB1	4SB1	3SB1	2SB1	LSB1
D7	D6	D5	D4	D3	D2	D1	D0
×	×	MSB2	5SB2	4SB2	3SB2	2SB2	LSB2

4. 7-bit ADPCM2 method

D15	D14	D13	D12	D11	D10	D9	D8
×	MSB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1
D7	D6	D5	D4	D3	D2	D1	D0
×	MSB2	6SB2	5SB2	4SB2	3SB2	2SB2	LSB2

5. 8-bit ADPCM2 method, 8-bit straight PCM method, and 8-bit non-linear PCM method

D15	D14	D13	D12	D11	D10	D9	D8
MSB1	7SB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1
D7	D6	D5	D4	D3	D2	D1	D0
MSB2	7SB2	6SB2	5SB2	4SB2	3SB2	2SB2	LSB2

6. 16-bit straight PCM method

D15	D14	D13	D12	D11	D10	D9	D8
MSB1	15SB1	14SB1	13SB1	12SB1	11SB1	10SB1	9SB1
D7	D6	D5	D4	D3	D2	D1	D0
8SB1	7SB1	6SB1	5SB1	4SB1	3SB1	2SB1	LSB1

FIFO Memory Configuration

The configuration of FIFO memory can be changed with command on the D7 to D0 pins. Select the FIFO memory taking bus length, monophonic/stereophonic playback models and buffering times into consideration. Initially, the FIFO memory is 512 bits (64 words by 8 bits).

Combination of FIFO memory capacity

(1) FIFO memory configuration when an 8-bit bus and monophonic reproduction are selected.
The following three FIFO memory sizes are selectable by commands :
1024 bits (128 words by 8 bits)
512 bits (64 words by 8 bits, initial value)
256 bits (32 words by 8 bits)

(2) FIFO memory configuration when 16-bit bus and monophonic reproduction are selected.
The following three FIFO memory sizes are selectable by commands :
1024 bits (64 words by 16 bits)
512 bits (32 words by 16 bits)
256 bits (16 words by 16 bits)

(3) FIFO memory configuration when an 8-bit bus and stereophonic reproduction are selected.
The following two FIFO memory sizes are selectable by commands :
512 bits (64 words by 8 bits) × 2
256 bits (32 words by 8 bits) × 2

(4) FIFO memory configuration when 16-bit bus and stereophonic reproduction are selected.
The following two FIFO memory sizes are selectable by commands :
512 bits (32 words by 16 bits) × 2
256 bits (16 words by 16 bits) × 2

Voice synthesis methods and maximum buffering times
When FIFO capacity of 1024 bits and sampling frequency of 8 kHz are selected :

	(Monophonic)	(Stereophonic)
(1) 8-bit bus selected		
4-bit ADPCM2 or ADPCM :	32 ms	16 ms
5-, 6-, 7-, and 8-bit ADPCM2 :	16 ms	8 ms
8-bit PCM :	16 ms	8 ms
(2) 16-bit bus selected	(Monophonic)	(Stereophonic)
16-bit PCM :	16 ms	8 ms

The other methods are the same as those when the 8-bit bus is used.

Playback operation (8-bit bus, 512-bit FIFO configuration)

(1) Voice synthesis, sampling frequency, bus length, and stereophonic playback modes can be set by commands. The FIFO memory is 64 words.

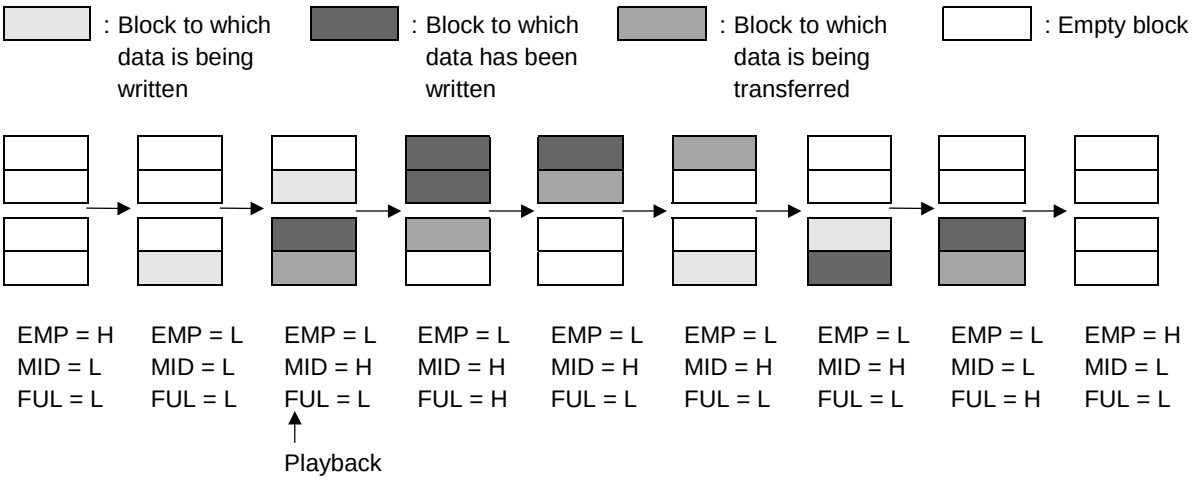
(2) When a Playback Start command is entered or when the EMP pin goes low (when data of 1 word is written in FIFO), the MSM9842 recognizes the start of playback and starts synthesizing voices when the MID pin goes high ("H").

(3) Status indication by EMP, MID, and FUL pins

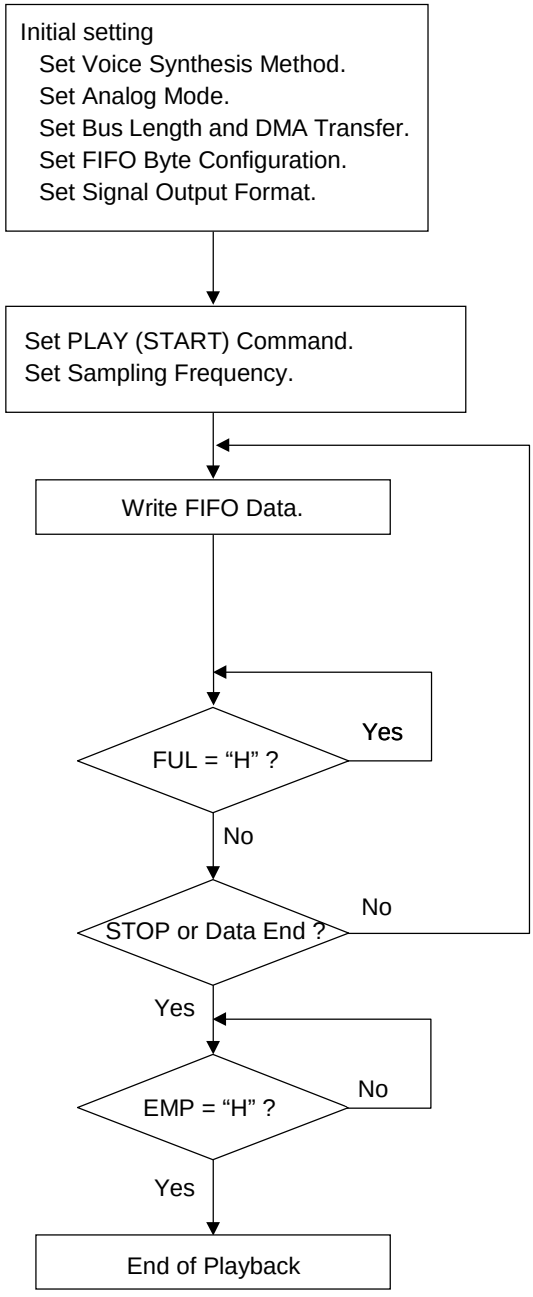
- EMP = "H", MID = "L", FUL = "L"
  No data is written in FIFO memory.
- EMP = "L", MID = "L", FUL = "L"
  Data of 1 word to 31 words has been written in FIFO memory. In this state, the data in the FIFO memory is not transferred to the voice synthesizer.
- EMP = "L", MID = "H", FUL = "L"
  Data of 32 words to 63 words has been written in FIFO memory. While the MID pin is "H", the data in the FIFO memory is not transferred to the voice synthesizer. If the MID and FUL pins fail to be set to "H", when the voice synthesizer has completed reading 32 words from FIFO, the MID pin goes low and the FUL pin goes high. In this state, the FIFO memory recognizes the end of playback and terminates the playback after transmitting the rest of data to the voice synthesizer.
- EMP = "L", MID = "H", FUL = "H"
  Data of 64 words is written in FIFO memory
  In this state, writing of 64 words into FIFO is completed before the voice synthesizer reads 32 words from FIFO and no data can be written in FIFO memory.

(4) End of playback
In the case of EMP = "L", MID = "H", and FUL = "L", if data is not written into the FIFO memory, playback is automatically terminated. Playback also can be terminated with the Stop command when reproducing the next phrase with a different sampling frequency. However, the FIFO memory data is cleared by input of the Stop command. The Stop command also can stop the playback on the way.

Change of FIFO memory status during playback



Playback Data Transfer Flowchart (without DMA transfer)



Note 1 : When the EMP pin is "H", transfer of all data is completed.

Note 2 : The MSM9842 supports two kinds of stop sequence : Forced stop with the STOP command and automatic stop after all date transfer is completed.

DMA Control Method

The MSM9842 sends a DMA Transfer request to the DMA controller and waits for a DMA transfer permission from the DMA controller. Upon reception of the permission, the MSM9842 starts data transfer at a transfer cycle of the DMA controller. The DMA Transfer function is enabled or disabled by commands.
Initially the DMA Transfer function is disabled.

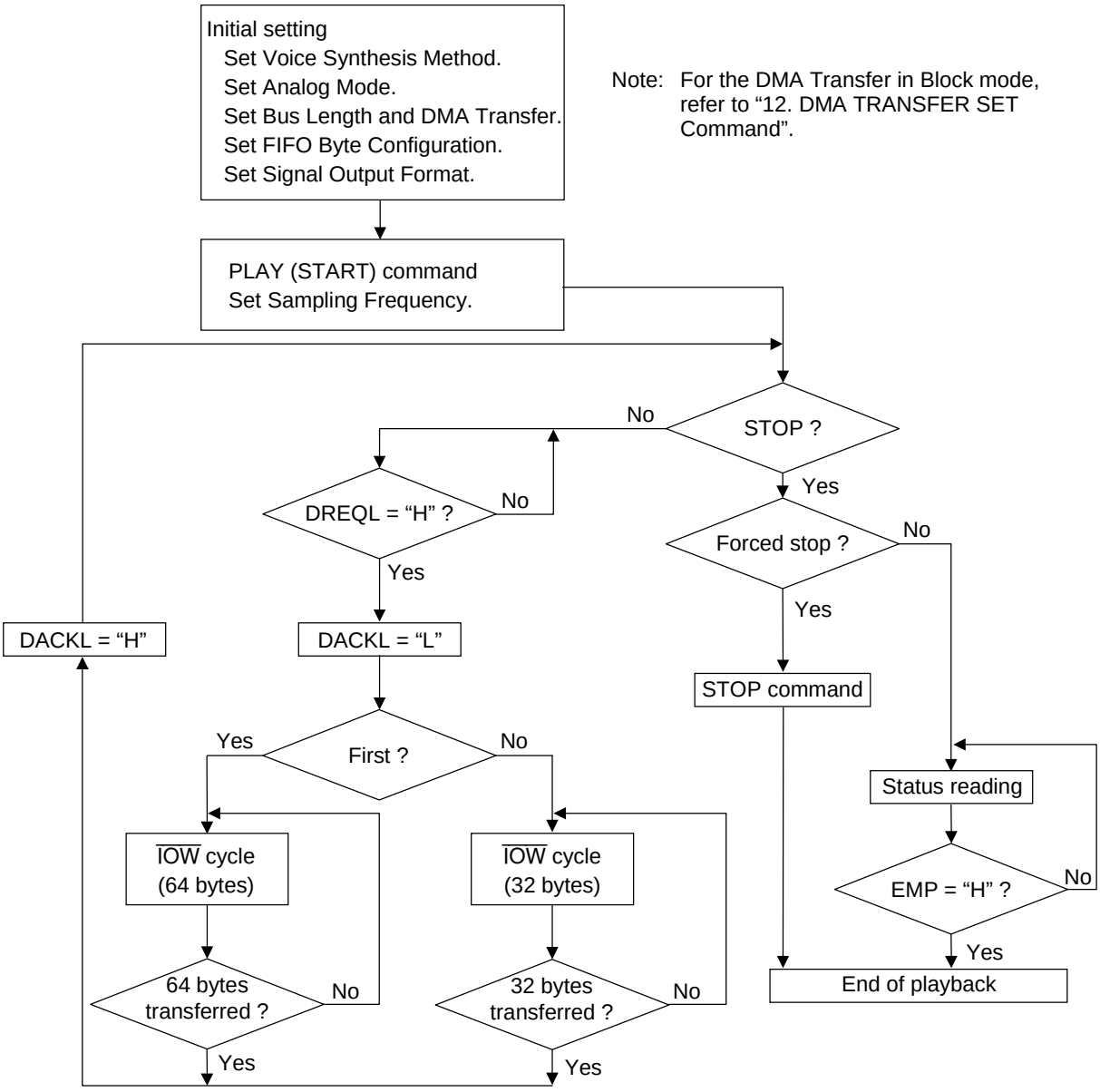
DREQL (8-bit bus, monophonic reproduction, 512-bit FIFO configuration)
This pin is used to send a DMA Transfer request to the DMA controller.

When the PLAY (START) command is entered, the DREQL pin goes high to request a cycle to write data into FIFO memory. After playback status, the DREQL pin remains high until the 64-word write cycle is completed. When a 32-word write cycle is completed, voice synthesis starts. From now on, each time the amount of data in FIFO memory becomes half, the DREQL pin goes high to send a 32-word DMA Transfer request.

DACKL and DACKR
These pins recognize a DMA Transfer acknowledge signal from the DMA controller.
When the DACKL/DACKR pin is at a low level ("L"), the $\overline{IOW}$ pin is enabled.
When the DACKL/DACKR pin is at a high level ("H"), control by the $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, and D/$\overline{C}$ pins is disabled. Therefore, all settings on the MSM9842 must be completed before the DMA transfer cycle starts.

$\overline{IOW}$
The $\overline{IOW}$ pin is enabled when the DACKL or DACKR pin goes low and their states are controlled by the DMA controller.
The $\overline{IOW}$ pin is an input pin to transfer data from external memory to the MSM9842.

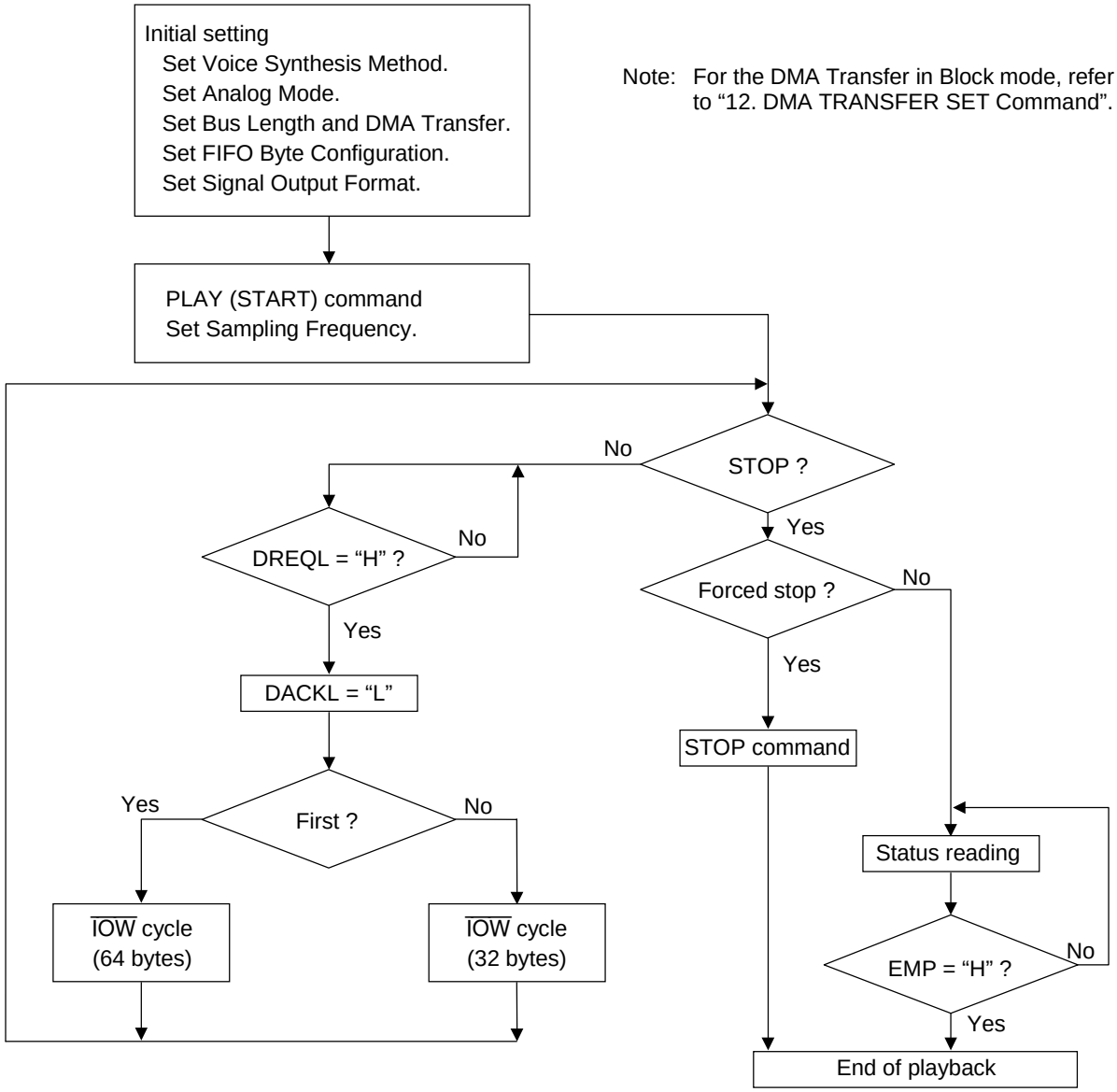
Playback Data Transfer Flowchart (with DMA transfer in Block mode)



Note 1 : The above flowchart assumes that FIFO memory is 64 bytes long. The MSM9842 writes data 64 bytes as a block in the first write-operation and writes a 32-byte block in the second and later write operations. A time period between the input of a DREQ request and the end of block writing depends upon a sampling frequency and the voice synthesis method. For example, when a 8 kHz sampling frequency and a 8-bit ADPCM2 voice synthesis method are set, a 32-byte block writing must be completed within 2 ms.

Note 2 : The MSM9842 supports two kinds of Playback Stop sequence: Forced stop by a STOP command and stop by status reading. When Playback is forcibly stopped by a STOP command, data in FIFO memory is all cleared. When status reading is made, Playback is stopped after all data left in FIFO memory is processed (EMP="H").

Playback Data Transfer Flowchart (with DMA transfer in Single mode)



Note: For the DMA Transfer in Block mode, refer to "12. DMA TRANSFER SET Command".

Playback Time and Memory Capacity

The playback time of the MSM9842 is dependent on the storage capacitance of external memory, the sampling frequency, and the length of ADPCM bits that has been specified. The playback time of the MSM9842 is expressed by

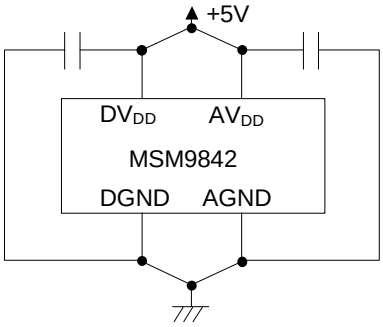
$$\text{Playback time} = \frac{1.024 \times \text{Memory capacity (K bit)}}{\text{Sampling frequency (kHz)} \times \text{bit length}} \text{ (seconds)}$$

For example, when 8.0 kHz of sampling frequency, 4 bit of ADPCM2, and 8M bit of memory size are set, the playback time is calculated as follows:

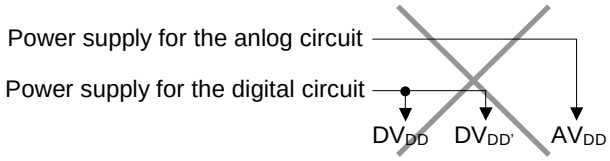
$$\text{Playback time} = \frac{1.024 \times 8000}{8.0 \times 4} = 256 \text{ (seconds)} = 4 \text{ minutes } 16 \text{ seconds}$$

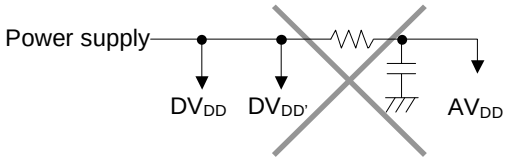
Connection of Power Supply

The MSM9842 contains a single power supply as shown below.
The power supply is connected to the analog unit and logic unit separately.



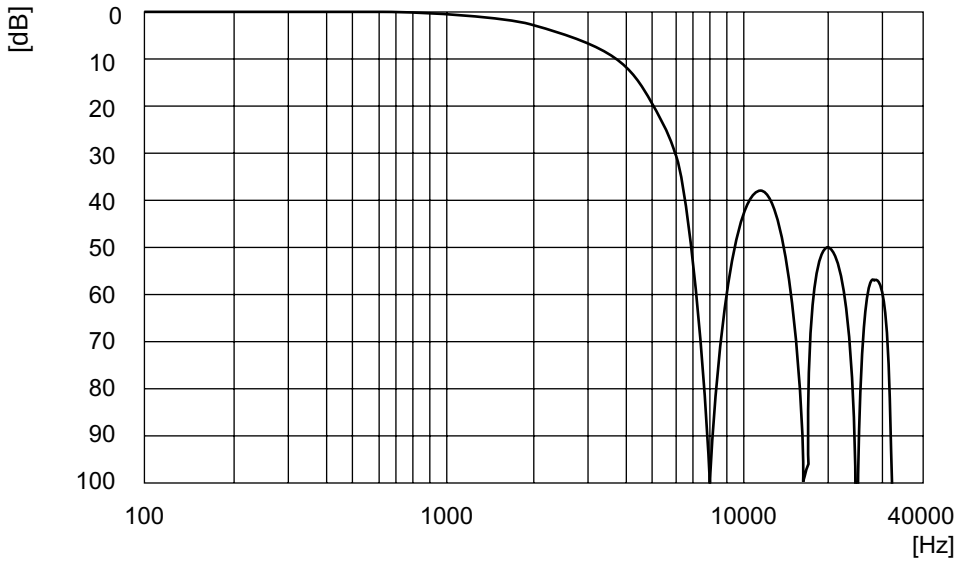
Avoid the following power supply connections:



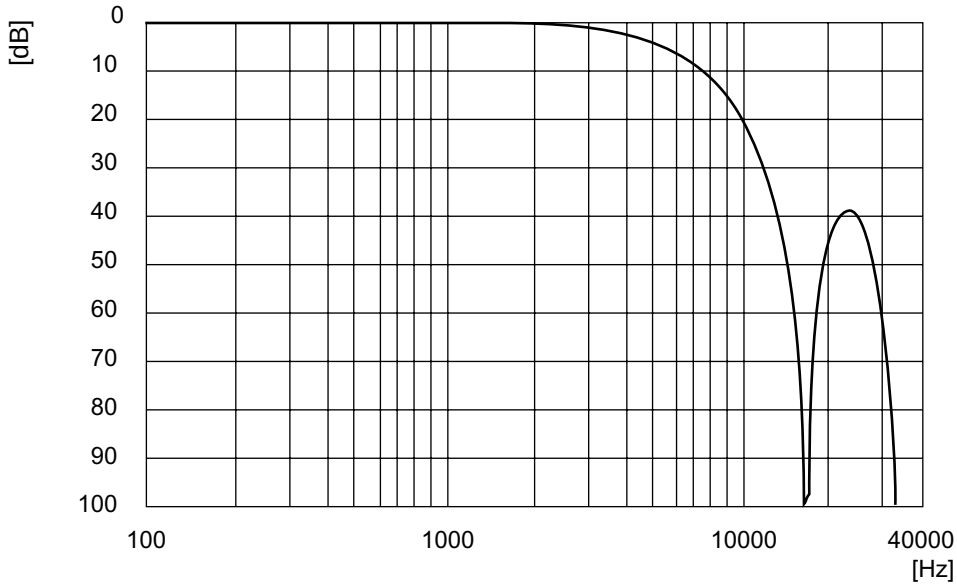


Frequency Characteristics of the Output Side LPF

The MSM9842 contains a line path filter (LPF) produced in the digital filter technology in the output of the DA converter during playback. Below are shown the frequency characteristics of the output side LPF (at fs = 8 kHz and 16 kHz).



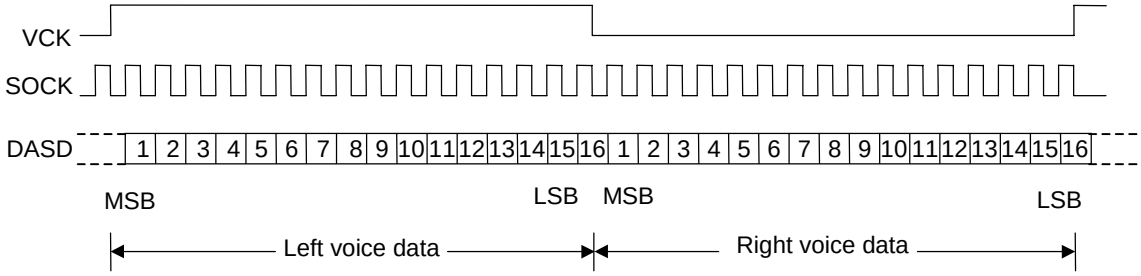
Frequency characteristics of the output side LPF (at fs = 8 kHz)



Frequency characteristics of the output side LPF (at fs = 16 kHz)

Using an External DAC

Select the External DAC mode and TOC or BIN by commands. The MSM9842 interfaces to the external DAC through the DASD, SOCK, and VCK pins. In monophonic playback, the MSM9842 outputs data when the VCK pin is at a high level ("H"). In stereophonic playback, the MSM9842 outputs left data when the VCK pin is at a high level ("H") and right data when the VCK pin is at a low level ("L"). The following figure shows stereophonic playback timing of the external DAC at a sampling frequency of 32 kHz (maximum).
Data is valid in back justification. Left voice data is valid if it is entered before the VCK signal falls. Right voice data is valid if it is entered before the VCK signal rises.



Stereophonic playback timing of the external DAC at VCK=32 kHz

COMMAND LIST

D7	D6	D5	D4	D3	D2	D1	D0	Function
0	0	0	0	0	0	0	0	No function
0	0	0	1	×	×	×	×	No function
0	0	1	0	H3	S2	S1	S0	PLAY START
0	0	1	1	C3	C2	×	×	STOP
0	1	0	0	C3	C2	C1	×	PAUSE
0	1	0	1	H3	V2	V1	V0	VOICE CONTROL
0	1	1	0	W3	W2	×	×	POWER-DOWN MODE
0	1	1	1	P3	P2	P1	P0	VOICE SYNTHESIS METHOD
1	0	0	0	R3	R2	×	R0	Analog specification 1
1	0	0	1	A3	A2	E1	E0	Analog specification 2 and bus length
1	0	1	0	×	0	B1	B0	FIFO memory configuration
1	0	1	1	F3	D2	D1	D0	Signal output format
1	1	0	0	G3	G2	G1	×	DMA Transfer

× = don't care

Voice Synthesis Method

P3	P2	P1	P0	Function	
0	0	0	0	4-bit Oki ADPCM2	*
0	0	0	1	5-bit Oki ADPCM2	
0	0	1	0	6-bit Oki ADPCM2	
0	0	1	1	7-bit Oki ADPCM2	
0	1	0	0	8-bit Oki ADPCM2	
0	1	0	1	4-bit Oki ADPCM	
0	1	1	0	8-bit PCM	
0	1	1	1	8-bit Oki non-linear PCM	
1	0	0	0	16-bit PCM	

Volume Setting

V2	V1	V0		
0	0	0	0 dB	*
0	0	1	–3 dB	
0	1	0	–6 dB	
0	1	1	–9 dB	
1	0	0	–12 dB	
1	0	1	–15 dB	
1	1	0	–18 dB	
1	1	1	–21 dB	

Sampling Frequency

S2	S1	S0	f_{SAM}	
0	0	0	8.0 kHz	*
0	0	1	12.8 kHz	
0	1	0	16.0 kHz	
0	1	1	32.0 kHz	
1	0	0	6.4 kHz	
1	0	1	4.0 kHz	

Voice Output Setting (1)

C3	C2	Function	
0	0	Left voice	*
1	0	Right voice	
×	1	Common to both left and right sides	

Voice Output Setting (2)

H3	Function	
0	Left voice	*
1	Right voice	

Pause Setting

C1	Function
0	Starts pausing
1	Cancels pausing

*: initial status

FIFO Memory Configuration

B1	B0	Function	
0	0	512 bit	*
0	1	1024 bit	
1	0	256 bit	
1	1	FIFO not used	

Note: Do not use in the stereophonic playback mode

Analog Specification 2 and Data Bus Transfer Setting

A3	Function	
0	With output amplifier	*
1	Without output amplifier	
A2	Function	
0	With LPF	*
1	Without LPF	
E1	Function	
0	8-bit bus length	*
1	16-bit bus length	
E0	Function	
0	D15 to D8 not used for 8-bit bus	*
1	D15 to D8 used for 8-bit bus	

Analog Specification 1

R3	Function	
0	Outputs in 2's complements.	*
1	Outputs in binary.	
R2	Function	
0	Uses internal DAC.	*
1	Uses external DAC.	
R0	Function	
0	Monophonic playback	*
1	Stereophonic playback	

Signal Output Format

F3	Function	
0	EMP, MID, and FUL outputs : Active high	*
1	EMP, MID, and FUL outputs : Active low	
D2	Function	
0	DREQL and DREQR outputs : Active high	*
1	DREQL and DREQR outputs : Active low	
D1	Function	
0	DACKL and DACKR outputs : Active low	*
1	DACKL and DACKR outputs : Active high	
D0	Function	
0	No function	*
1	For testing. Don't use	

Power-down Setting

W3	Function	
0	Cancels power-down.	*
1	Starts power-down.	
W2	Function	
0	Retains LSI internal setting.	*
1	Initializes LSI internal setting.	

DMA Transfer Setting

G3	G2	G1	Function	
0	×	×	Without DMA transfer	*
1	0	0	Single mode transfer	
1	0	1	Block mode transfer	

*: initial status

Description of Commands

1. NOP command

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0
0	0	0	1	×	×	×	×

No function

2. PLAYBACK command

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	C3	S2	S1	S0

This command starts playback. Bits D2 to D0 specify a sampling frequency. Bit D3 selects left or right voice data to be played back. In the continuous monophonic playback with a different sampling frequency, be sure to enter the STOP command before starting playback of the next phrase.
For stereophonic playback, left and right sampling frequencies must be the same.

C3	Function	
0	Playback of left voice	*
1	Playback of right voice	

S2	S1	S0	Sampling frequency	
			f_{OSC} = 4.096 MHz	f_{OSC} = 5.6448 MHz
0	0	1	**8.0 kHz** *	11.03 kHz
0	0	1	**12.8 kHz**	17.64 kHz
0	1	0	**16.0 kHz**	**22.05 kHz**
0	1	1	**32.0 kHz**	**44.1 kHz**
1	0	0	**6.4 kHz**	8.82 kHz
1	0	1	**4.0 kHz**	5.51 kHz

*: initial status

3. STOP command

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	C3	C2	×	×

In the playback mode, this command aborts playback. When this command is entered, data in FIFO memory is cleared. Bit D3 selects left or right voice whose playback is aborted.
Turn on bit D2 to abort playback of both left and right voices at a time.

C3	C2	Function
0	0	Aborts playback of left voice.
1	0	Aborts playback of right voice.
×	1	Aborts playback of left and right voices.

4. PAUSE command

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	C3	C2	C1	×

This command pauses the current playback operation. Bit D1 enables or disables pausing.
When playback is paused, bit D3 selects left or right voice whose playback is paused. Turn on bit D2 to pause playback of both left and right voices.

C1	Function
0	Starts pausing.
1	Cancels pausing.

C3	C2	Function
0	0	Pauses playback of left voice.
1	0	Pauses playback of right voice.
×	1	Pauses playback of both left and right voices.

5. VOLUME command

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	C3	V2	V1	V0

This command controls the volume of playback voices.
Bit D3 selects a left or right voice to be volume-controlled during playback. Bits D2 to D0 set the volume.

C3	Function
0	Sets the volume of left voice.
1	Sets the volume of right voice.

V2	V1	V0	Volume	
0	0	0	0 dB	*
0	0	1	–3 dB	
0	1	0	–6 dB	
0	1	1	–9 dB	
1	0	0	–12 dB	
1	0	1	–15 dB	
1	1	0	–18 dB	
1	1	1	–21 dB	

6. POWER-DOWN command

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	W3	W2	×	×

When receiving this command, the MSM9842 stops oscillation, minimizes the current consumption, and enters the power-down status. The AOUTL and AOUTR outputs immediately fall to the GND level. Bit D3 enables or disables the power-down function and bit D2 enables or disables initialization of the internal circuit of the MSM9842.

W3	Function
0	Disables the power-down function.
1	Enables the power-down function.

W2	Function
0	Disables initialization of the internal circuit of the LSI.
1	Enables initialization of the internal circuit of the LSI.

*: initial status

7. VOICE SYNTHESIS METHOD command

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	P3	P2	P1	P0

This command selects a voice synthesis method. Bits D3 to D0 select a method. A total of nine voice synthesis methods are selectable. The selected voice synthesis method cannot be changed while playback is in progress.

P3	P2	P1	P0	Voice synthesis method	
0	0	0	0	4-bit ADPCM2	*
0	0	0	1	5-bit ADPCM2	
0	0	1	0	6-bit ADPCM2	
0	0	1	1	7-bit ADPCM2	
0	1	0	0	8-bit ADPCM2	
0	1	0	1	4-bit ADPCM	
0	1	1	0	8-bit straight PCM	
0	1	1	1	8-bit non-linear PCM	
1	0	0	0	16-bit straight PCM	

8. ANALOG SPECIFICATION 1 command

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	R3	R2	×	R0

× = don't care

This command selects the built-in DAC, the external DAC, indication of 2's complement or binary, and stereophonic or monophonic playback. When the MSM9842 is turned on, the AOUTL and AOUTR pin voltages immediately rise to 1/2 V_{DD}.

R3	Function	
0	2's complement when external DAC is selected	*
1	Binary when external DAC is selected	

R2	Function	
0	Internal DAC	*
1	External DAC	

R0	Function	
0	Monophonic playback mode	*
1	Stereophonic playback mode	

*: initial status

9. ANALOG SPECIFICATION DATA BUS LENGTH SET command

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	A3	A2	E1	E0

D3 selects use or disuse of the internal output amplifiers to the AOUTL Pin and the AOUTR Pin. D2 selects use or disuse of the internal LPFs to the AOUTL Pin and the AOUTR Pin.
D1 and D0 set a data bus length and select use or disuse of D15 to D8 for voice data transfer when the 8-bit bus is selected. D1 and D0 select "D15 to D8 not used for 8-bit bus length" when D7 to D0 pins are used to transfer (input or output) all data including commands, status, and data. D1 and D0 select "D15 to D8 used for 8-bit bus length" when D15 to D8 pins are used to input or output data and D7 to D0 pins are used to input or output commands and statuses.

A3	Function	
0	With output amplifier	*
1	Without output amplifier	

A2	Function	
0	With LPF	*
1	Without LPF	

E1	E0	Function	
0	0	D15 to D8 not used for 8-bit bus length	*
0	1	D15 to D8 used for 8-bit bus length	
1	×	16-bit bus length	

*: initial status

10. FIFO MEMORY SPECIFICATION command

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	×	0	B1	B0

This command selects a bit configuration (word configuration) of the FIFO memory. When stereophonic playback is selected, this command selects a left side or right side bit configuration (word configuration). Therefore, the 1024-bit configuration can not be selected because the MSM9842 contains 1024 bits of FIFO memory.

	B1	B0	8-bit bus configuration	16-bit bus configuration
*	0	0	512 bits (64 words)	512 bits (32 words)
Note	0	1	1024 bits (128 words)	1024 bits (64 words)
	1	0	256 bits (32 words)	256 bits (16 words)
	1	1	FIFO memory not used	

Note: For stereophonic playback, the word configuration cannot be selected.

* : initial status

11. SIGNAL OUTPUT FORMAT CONTROL command

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	F3	D2	D1	D0

This command sets the output formats of the EMP, MID, FUL, DREQL, and DREQR pins and the input formats of the DACKL and DACKR pins.

F3	Function	
0	EMP, MID, FUL outputs : Active high	*
1	EMP, MID, FUL outputs : Active low	

D2	Function	
0	DREQL and DREQR outputs : Active high	*
1	DREQL and DREQR outputs : Active low	

D1	Function	
0	DACKL and DACKR inputs : Active low	*
1	DACKL and DACKR inputs : Active high	

D0	Function
0	No function
1	For test. Not used

12. DMA TRANSFER SET Command

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	G3	G2	G1	×

This command sets use or disuse of DMA transfer or selects DMA transfer mode. When the Single mode DMA transfer is selected, the DREQL pin or DREQR pin (when stereophonic playback is selected) is active while DMA transfer is being requested. The Single mode DMA transfer is selected when transferring data monitoring the status of the DREQL or DREQR pin without controlling the number of bytes to be transferred. When the Block mode DMA transfer is selected, the DREQL pin or DREQR pin (when stereophonic playback is selected) sends a DMA request signal and becomes inactive when the DACKL pin or DACKR pin is active. The Block mode DMA transfer is selected when the number of bytes to be transferred can be controlled and the DREQL or DREQR pin is set to be inactive.

G3	G2	G1	Function	
0	×	×	Without DMA transfer	*
1	0	0	Single mode DMA transfer	
1	0	1	Block mode DMA transfer	

*: initial status

Description of Status

The MSM9842 supports the following seven status flags :

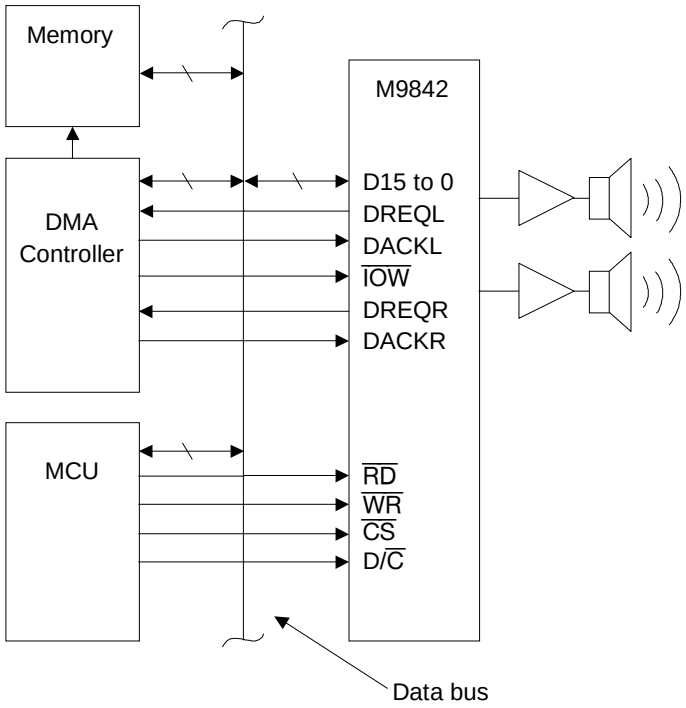
D7	Left Data Playing flag	High when playback is in progress
D6	Right Data Playing flag	High when playback is in progress
D5	Left Pause flag	High when playback of left voice is paused
D4	Right Pause flag	High when playback of right voice is paused
D3	EMP Information Output flag	Output the same signal as the EMP pin. Note
D2	MID Information Output flag	Output the same signal as the MID pin. Note
D1	FUL Information Output flag	Output the same signal as the FUL pin. Note
D0	Data Transfer Error flag	See the explanation below.

Note: The EMP, MID and FUL pins output active high signals.
The signal output format cannot be specified by a command.

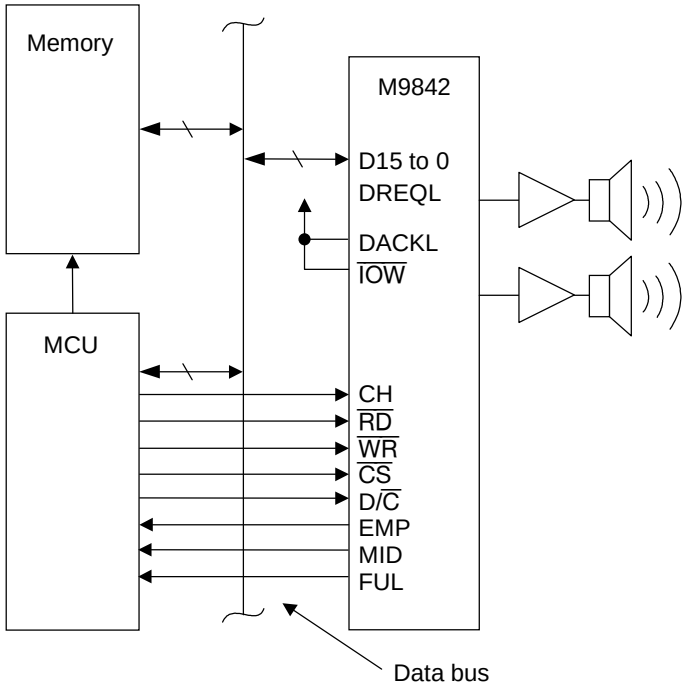
The MSM9842 supports the following two data transfer errors :
When FIFO memory is used
(1) “H” when a read operation is made while EMP is “H”
(2) “H” when a write operation is made while FUL is “H”

CPU INTERFACE EXAMPLES

1) Interface when DMA controller is used (16-bit bus)



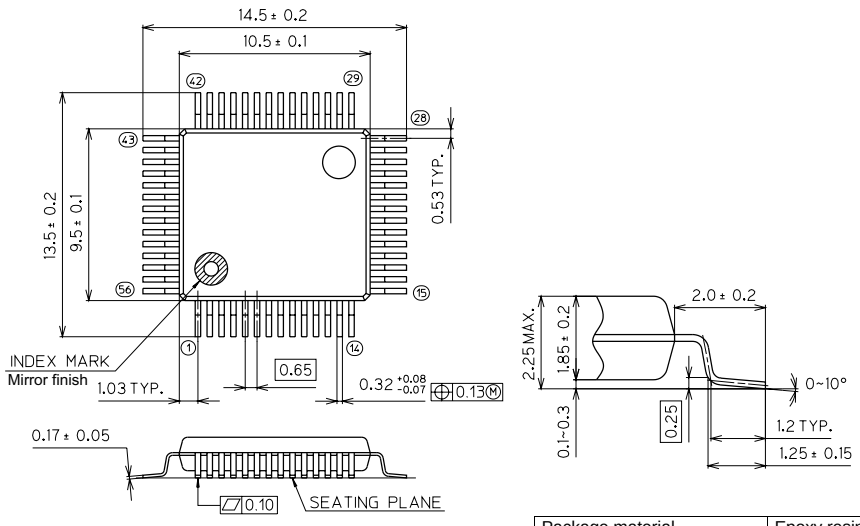
2) MCU & external memory interface (16-bit bus)



PACKAGE DIMENSIONS

(Unit: mm)

QFP56-P-910-0.65-2K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.43 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

3. When designing your product, please use our product below the specified maximum ratings and within the specified operating ranges including, but not limited to, operating voltage, power dissipation, and operating temperature.

4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.

5. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.

6. The products listed in this document are intended for use in general electronics equipment for commercial applications (e.g., office automation, communication equipment, measurement equipment, consumer electronics, etc.). These products are not authorized for use in any system or application that requires special or enhanced quality and reliability characteristics nor in any system or application where the failure of such system or application may result in the loss or damage of property, or death or injury to humans.
   Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.

7. Certain products in this document may need government approval before they can be exported to particular countries. The purchaser assumes the responsibility of determining the legality of export of these products and will take appropriate and necessary steps at their own expense for these.

8. No part of the contents contained herein may be reprinted or reproduced without our prior permission.