OKI Semiconductor

FEDL9802-03-05-06
Issue Date: Nov. 22, 2004

MSM9802/03/05-xxx

Voice Synthesis IC with Built-in Mask ROM

GENERAL DESCRIPTION

The MSM9802/03/05 is a PCM voice synthesis IC with built-in mask ROM.
This IC has two user selectable playback algorithms, OKI Non-linear PCM and straight PCM. It also contains a current mode 10-bit D/A converter and a low-pass filter.
External control has been made easy by the built-in edit ROM that can form sentences by linking phrases. By using Oki's Sound Analysis and Editing Tool, ROM data such as Phrase Control Table can be easily set, created, edited, and evaluated.
With the stand-alone mode/microcontroller interface mode switching pin, the MSM9802/03/05 can support various applications.

FEATURES

Device	ROM size*	Speech period (sec)			
		f_{SAM} = 4.0kHz	f_{SAM} = 6.4kHz	f_{SAM} = 8.0kHz	f_{SAM} = 16.0kHz
MSM9802	512Kbits	16.0	10.0	8.0	4.0
MSM9803	1Mbit	32.4	20.2	16.2	8.1
MSM9805	2Mbits	65.1	40.7	32.5	16.2

* Actual voice ROM area is smaller by 11 Kbits.

- ROM custom
- 8-bit OKI nonlinear PCM method/8-bit straight PCM method
- Built-in edit ROM
- Random playback function
- Sampling frequency : 4.0 kHz/5.3 kHz/6.4 kHz/8.0 kHz/10.6 kHz/12.8 kHz/16.0 kHz
  Note: If RC oscillation is selected, 10.6 kHz, 12.8 kHz, and 16.0 kHz cannot be selected.
- Maximum number of phrases : 63 (Microcontroller interface mode)
  56 (Stand-alone mode)
- Built-in current mode 10-bit D/A converter
- Built-in low-pass filter
- Standby function
- RC oscillation (256 kHz)/ceramic oscillation (4.096 MHz) selectable
- Package options:

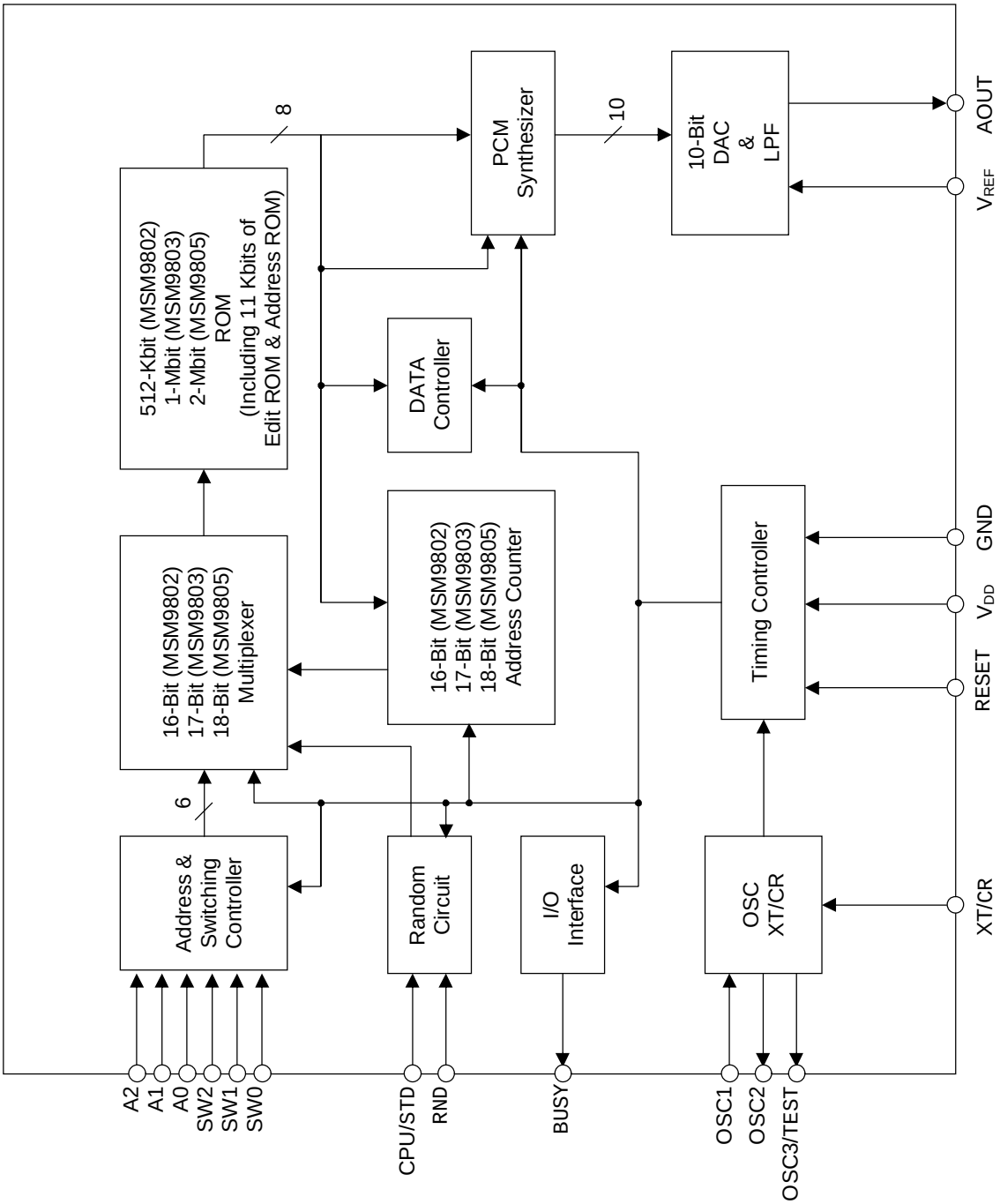
18-pin plastic DIP	(DIP18-P-300-2.54)	(MSM9802-xxxRS/MSM9803-xxxRS/ MSM9805-xxxRS)
24-pin plastic SOP	(SOP24-P-430-1.27-K)	(MSM9802-xxxGS-K/MSM9803-xxxGS-K/ MSM9805-xxxGS-K)
30-pin plastic SSOP	(SSOP30-P-56-0.65-K)	(MSM9802-xxxGS-AK/MSM9803-xxxGS-AK/ MSM9805-xxxGS-AK)
Chip		xxx indicates code number.

Note: This data sheet explains a stand-alone mode and a microcontroller interface mode, separately.

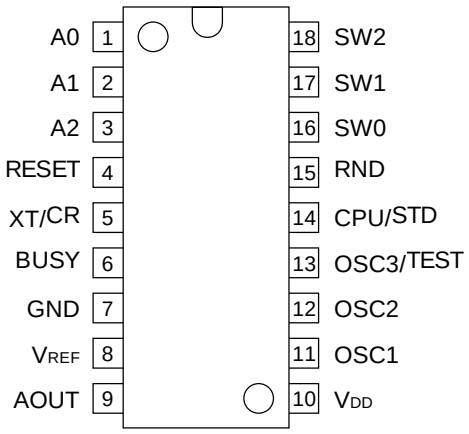
CONTENTS

(1) STAND-ALONE MODE (CPU/STD: "L" LEVEL)

BLOCK DIAGRAM

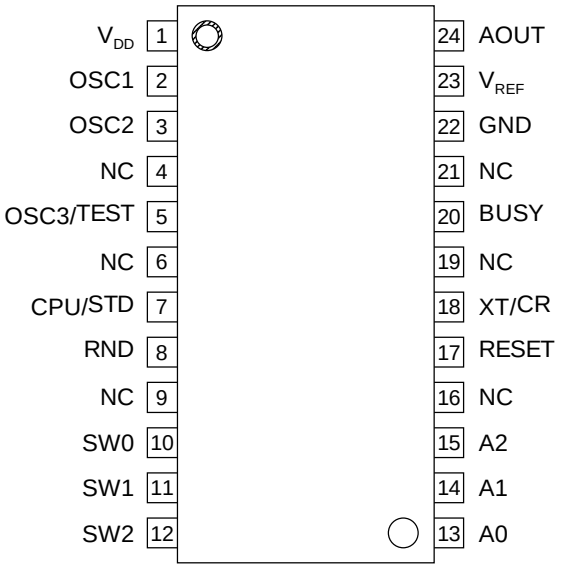


PIN CONFIGURATION (TOP VIEW)



18-Pin Plastic DIP

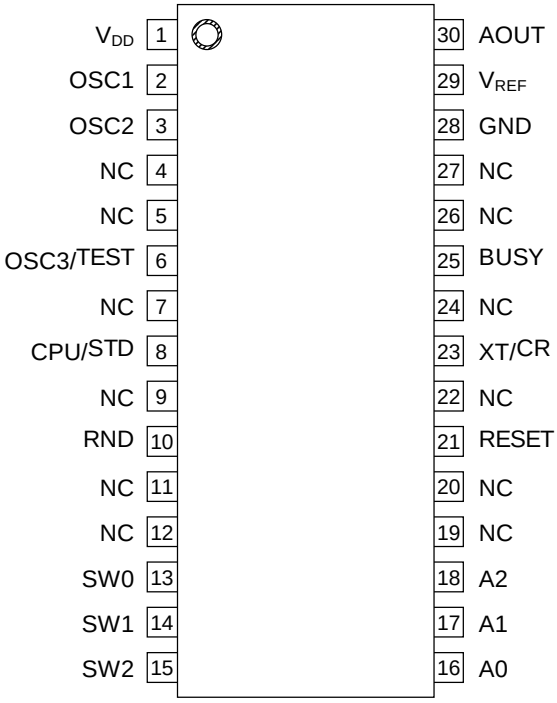
Note: Applicable to MSM9802-xxxRS, MSM9803-xxxRS, and MSM9805-xxxRS.



NC: No connection

24-Pin Plastic SOP

Note: Applicable to MSM9802-xxxGS-K, MSM9803-xxxGS-K, and MSM9805-xxxGS-K.



NC: No connection

30-Pin Plastic SSOP

Note: Applicable to MSM9802-xxxGS-AK, MSM9803-xxxGS-AK, and MSM9805-xxxGS-AK.

PIN DESCRIPTIONS

Pin			Symbol	Type	Description
DIP	SOP	SSOP			
4	17	21	RESET	I	The IC enters the standby state if this pin is set to “L” level. At this time, oscillation stops and AOUT drives a current of 0mA and becomes GND level, then the IC returns to the initial state. Apply a “L” pulse upon power-on. This pin has an internal pull-up resistor.
6	20	25	BUSY	O	Outputs “L” level while voice is being played back. At power-on, this pin is at “H” level.
5	18	23	XT/CR	I	XT/RC switching pin. Set to “H” level if ceramic oscillation is used. Set to “L” level if RC oscillation is used.
14	7	8	CPU/STD	I	Microcontroller interface/stand-alone mode switching pin. Set to “L” level if the MSM9802/03/05 is used in stand-alone mode.
8	23	29	V_{REF}	I	Volume setting pin. If this pin is set to GND level, the maximum current is forced in. If this pin is set to V_{DD} level, the minimum current is forced in. A pull-down resistor of approx. 10Ω is internally connected to this pin during operation.
9	24	30	AOUT	O	Voice output pin. The voice signals are output as current changes. In standby state, this pin drives a current of 0 mA and becomes GND level.
7	22	28	GND	—	Ground pin.
10	1	1	V_{DD}	—	Power supply pin. Insert a bypass capacitor of 0.1 µF or more between V_{DD} and GND pins.
11	2	2	OSC1	I	Ceramic oscillator connection pin when ceramic oscillation is selected. RC connection pin when RC oscillation is selected. Input from this pin if external clock is used.
12	3	3	OSC2	O	Ceramic oscillator connection pin when ceramic oscillation is selected. RC connection pin when RC oscillation is selected. Leave this pin open if external clock is used. Outputs “L” level in standby state.
13	5	6	OSC3/TEST	O	Leave this pin open when ceramic oscillation is used. RC connection pin when RC oscillation is selected. Outputs “H” level in standby state when RC oscillation is selected.
15	8	10	RND	I	Random playback starts if RND pin is set to “L” level. Fetches addresses from random address generation circuit in the IC at fall of RND. Set to “H” level when the random playback function is not used. This pin has internal pull-up resistor.

Pin			Symbol	Type	Description
DIP	SOP	SSOP			
16-18	10-12	13-15	SW0-SW2	I	Phrase input pins corresponding to playback sound. If input changes, SW0 to SW2 pins fetch addresses after 16 ms and start voice synthesis. Each of these pins has internal pull-down resistor.
1-3	13-15	16-18	A0-A2	I	Phrase input pins corresponding to playback sound. Input logic of A0 pin becomes invalid if the random playback function is used.

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +7.0	V
Input Voltage	V_{IN}		–0.3 to + V_{DD} +0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V)

Parameter	Symbol	Condition	Rating			Unit
Power Supply Voltage	V_{DD}	—	2.0 to 5.5			V
Operating Temperature	T_{op}	—	–40 to +85			°C
Master Clock Frequency 1	f_{OSC1}	When crystal is selected	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	
Master Clock Frequency 2	f_{OSC2}	When RC is selected (*1)	200	256	300	kHz

*1 The accuracy of the oscillation frequency when RC oscillation is selected depends largely on the accuracy of the external R and C.

ELECTRICAL CHARACTERISTICS

DC Characteristics (1)

(V_{DD} = 5.0 V, GND = 0 V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	4.2	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.8	V
"H" Output Voltage	V_{OH}	I_{OH} = –1 mA	4.6	—	—	V
"L" Output Voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V
"H" Input Current 1	I_{IH1}	$V_{IH} = V_{DD}$	—	—	10	µA
"H" Input Current 2 *1	I_{IH2}	Internal pull-down resistor	30	90	200	µA
"H" Input Current 3	I_{IH3}	Applies to OSC1 pin only. $V_{IH} = V_{DD}$	—	—	15	µA
"L" Input Current 1	I_{IL1}	V_{IL} = GND	–10	—	—	µA
"L" Input Current 2 *2	I_{IL2}	Internal pull-up resistor	–200	–90	–30	µA
Dynamic Supply Current 1 *3	I_{DD1}	$V_{REF} = V_{DD}$, AOUT bias voltage = 0V	—	0.4	1	mA
Dynamic Supply Current 2 *4	I_{DD2}	At maximum output current V_{REF} = GND, AOUT bias voltage = 0V	—	—	16	mA
Standby Current	I_{DS}	Ta = –40 to +70°C	—	—	10	µA
		Ta = 70 to 85°C	—	—	50	µA
AOUT Output Current	I_{AOUT}	At maximum output current, V_{REF} = GND, AOUT bias voltage = 0V	6	9.5	15	mA
V_{REF} Pin Pull-down Resistance	R_{VREF}	—	7	10	13	kΩ

*1 Applicable to SW0-SW2
*2 Applicable to RESET, RND
*3 Dynamic supply current (excluding DAC output current)
*4 Dynamic supply current at maximum output current

DC Characteristics (2)

(V_{DD} = 3.1 V, GND = 0 V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	2.7	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.5	V
"H" Output Voltage	V_{OH}	I_{OH} = –1 mA	2.6	—	—	V
"L" Output Voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V
"H" Input Current 1	I_{IH1}	$V_{IH} = V_{DD}$	—	—	10	µA
"H" Input Current 2 *1	I_{IH2}	Internal pull-down resistor	10	30	100	µA
"H" Input Current 3	I_{IH3}	Applies to OSC1 pin only. $V_{IH} = V_{DD}$	—	—	15	µA
"L" Input Current 1	I_{IL1}	V_{IL} = GND	–10	—	—	µA
"L" Input Current 2 *2	I_{IL2}	Internal pull-up resistor	–100	–30	–10	µA
Dynamic Supply Current 1 *3	I_{DD1}	$V_{REF} = V_{DD}$, AOUT bias voltage = 0V	—	0.15	0.5	mA
Dynamic Supply Current 2 *4	I_{DD2}	At maximum output current V_{REF} = GND, AOUT bias voltage = 0V	—	—	5.5	mA
Standby Current	I_{DS}	Ta = –40 to +70°C	—	—	5	µA
		Ta = 70 to 85°C	—	—	20	µA
AOUT Output Current	I_{AOUT}	At maximum output current, V_{REF} = GND, AOUT bias voltage = 0V	1.4	3.2	5	mA
V_{REF} Pin Pull-down Resistance	R_{VREF}	—	7	10	13	kΩ

*1 Applicable to SW2-SW0
*2 Applicable to RESET, RND
*3 Dynamic supply current (excluding DAC output current)
*4 Dynamic supply current at maximum output current

AC Characteristics

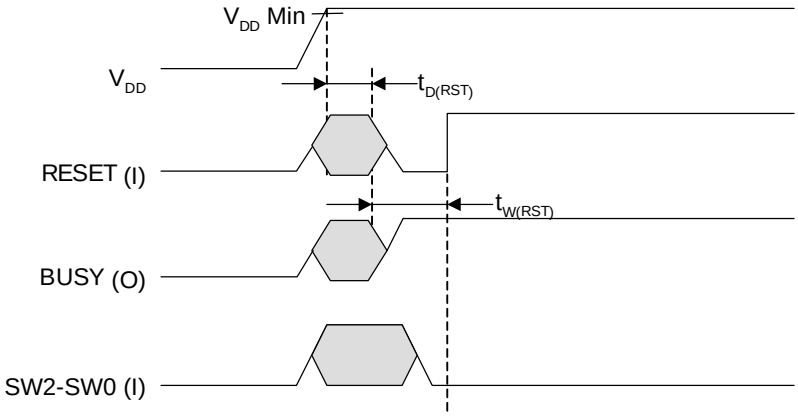
(V_{DD} = 5.0 V, GND = 0 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Master Clock Duty Cycle	f_{duty}	—	40	50	60	%
RESET Input Pulse Width	$t_{w(RST)}$	—	10	—	—	µs
RESET Input Time After Power-on	$t_{D(RST)}$	—	0	—	—	µs
RND Input Pulse Width	$t_{w(RAN)}$	—	100	—	—	µs
SW0-SW2 Input Pulse Width	$t_{w(SW)}$	— (note)	16	—	—	ms
BUSY Output Time	t_{SBS}	—	—	—	10	µs
Chattering Prevention Time 1	t_{CHA}	— (note)	14	15	16	ms
Chattering Prevention Time 2	t_{CHB}	— (note)	—	—	16	ms
D/A Converter Change Time	t_{DAR}, t_{DAF}	— (note)	60	64	68	ms
Standby Transition Time	t_{STB}	— (note)	200	250	300	ms
Silence Time Between Phrases	t_{BLN}	f_{SAM} = 8 kHz (note)	350	375	500	µs
Random Address Fetch Time	t_{RA}	— (note)	15	16	17	µs

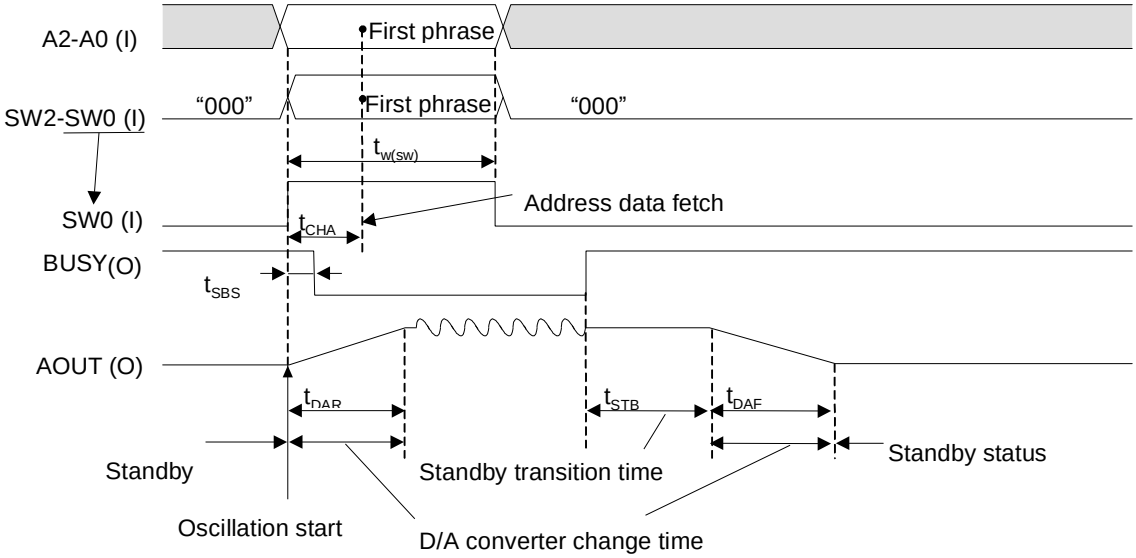
(Note) Proportional to master the periods of oscillation frequencies f_{OSC1} and f_{OSC2}.
The rated values show values when the standard master oscillation frequency is used.

TIMING DIAGRAMS

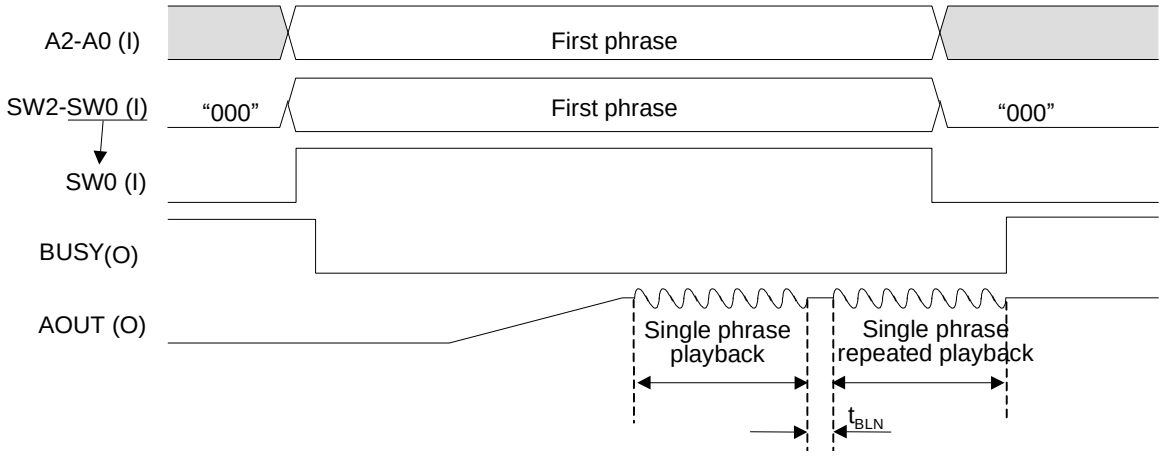
AC Characteristics at Power-On



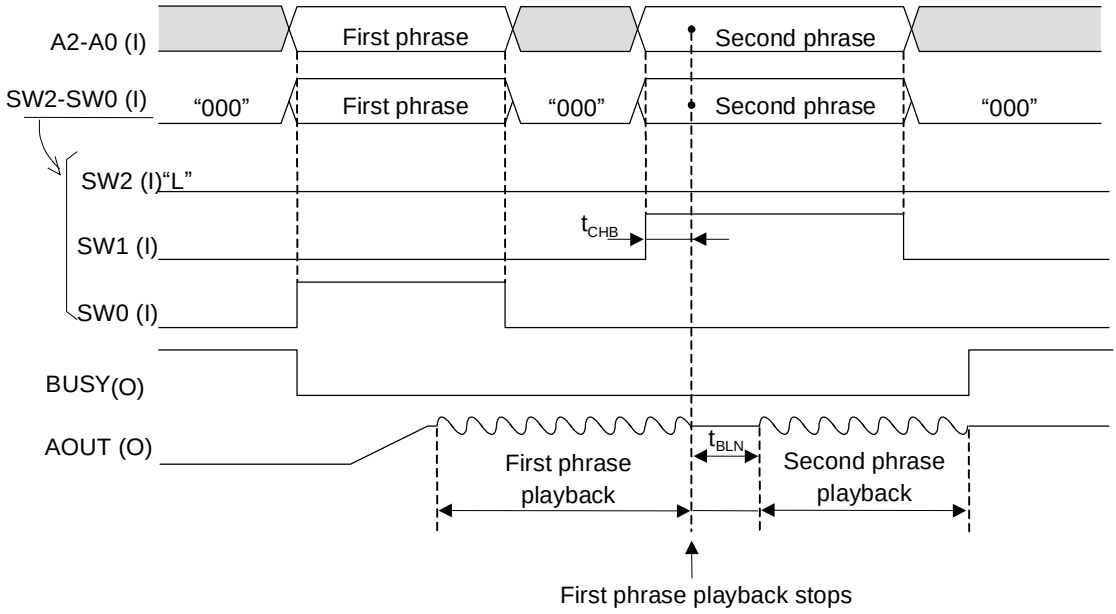
AC Characteristics in Standby Status and when the IC is Activated



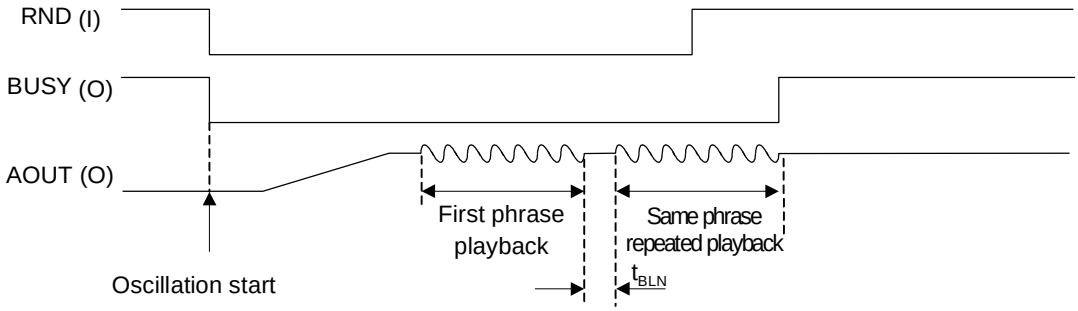
Repeated Playback Timing



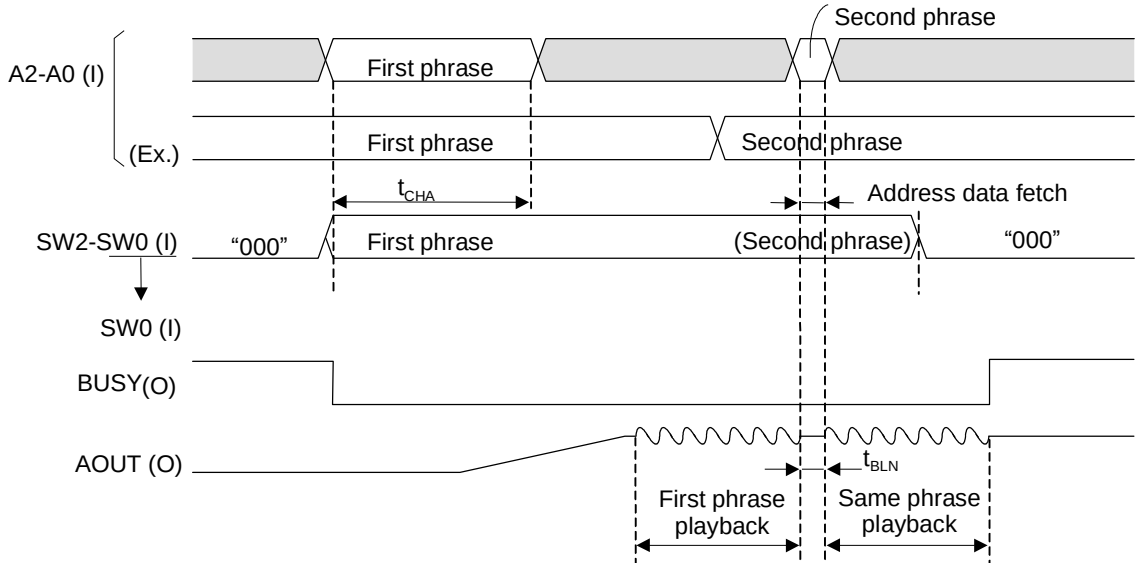
Timing when Changing from SW2 to SW0 During Playback



Repeated Playback Timing for Random Playback



Timing when Changing from A2 to A0 During Playback



FUNCTIONAL DESCRIPTION

Playback Code Specification

The user can specify a maximum of 56 phrases. Table 1.1 shows the settings by the A2-A0 and SW2-SW0 pins.

Table 1.1 User-specified Phrases

A2-A0	SW2-SW0	Code Details
000	000	Inhibit code
⋮	001 ⋮	User-specified phrase (56 phrases)
111	111	

Pull-up/Pull-down Resistor

The RESET and RND pins have internal pull-up resistors and the SW2-SW0 pins have internal pull-down resistors.

Stand-alone Mode

In a stand-alone mode, the SW input interface function and the random playback function can be used.

SW input interface

With the SW input interface, speech synthesis starts when the state of the SW2-SW0 pins has changed. To prevent chattering, the address data is latched 16 ms (t_{CHA}) after the state of SW2-SW0 has changed. Voice synthesis does not start if the state of the A2-A0 pins has changed. Set the RND pin to "H" level if the random playback function is not used.

Set the A2-A0 pins to "L" level at power-on or at reset.
The SW input interface is effective when the MSM9802/03/05 is operated using a push-button switch. Voice synthesis starts when an address is changed by pressing the push-button switch. If the push-button switch is released during playback, then playback stops after the current phrase is completed.

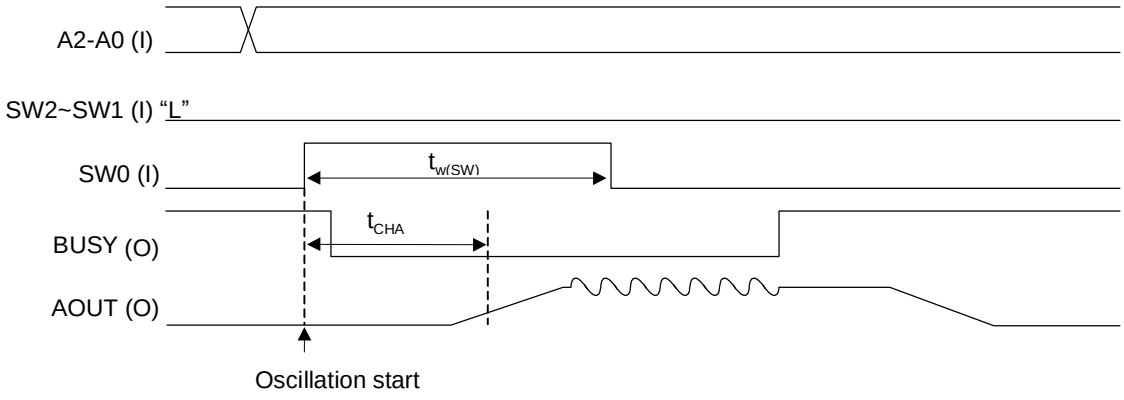


Figure 3.1 SW Input Interface Single-Phrase Playback Timing

If playback is attempted at an unused address in the phrases, AOUT goes to 1/2 I_{AOUT} and playback does not occur. Figure 3.2 shows the timing.

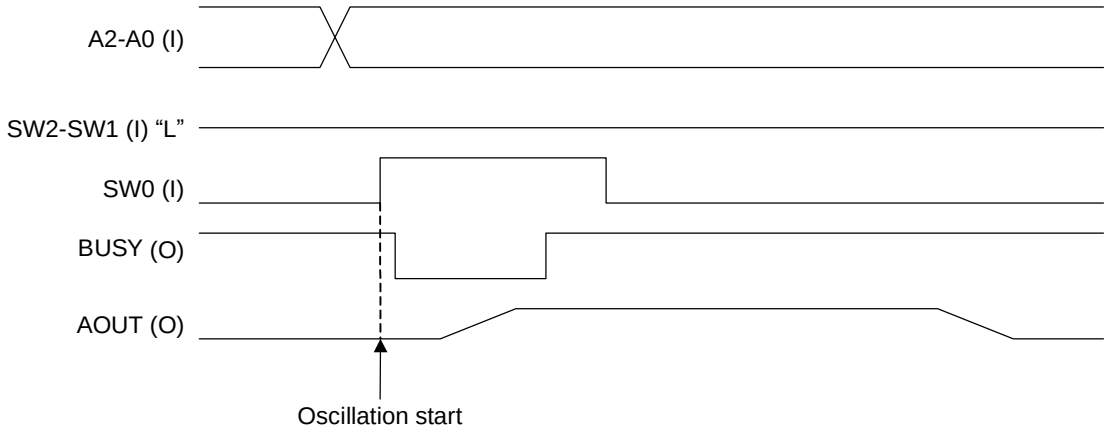
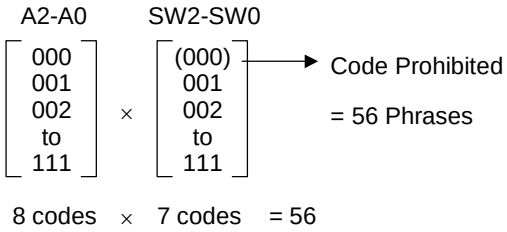


Figure 3.2 Timing when Playback is Attempted at an Unused Phrase Address

In the SW input interface, no phrase is triggered when SW2 to SW0 are all set to "0". Therefore, when the circuit consists of a diode matrices that use push-button switches, the maximum playback phrases are 56 phrases.



Random playback function

The random playback function randomly generates 15 different addresses corresponding to the four bits of the addresses of A0 and SW2-SW0 (except ALL "L") on the IC, after which playback commences.

Therefore, any input to A0 and SW2 to SW0 pins from external control is invalid. Hold these 4 pins either "H" or "L" level. SW2 to SW0 pins may be held open as they have internal pull-down resistor.

Playback may not occur if all the 15 addresses have not been assigned a phrase. Care must be taken when creating ROM data.

For example, when four phrases, "sunny", "rainy", "cloudy", and "snowy", are to be played randomly, set the phrases as shown in Table 3.1 in which a phrase is assigned to all the 15 addresses. The four phrases are then played back at random as shown below.

Table 3.1 Random Address Setup Example

A2, A1	A0, SW2-SW0	Phrase
00	0001	sunny
	0010	rainy
	0011	cloudy
	0100	snowy
	0101	sunny
	1110	rainy
	1111	snowy

Random playback starts when the timing shown in Figure 3.3 is input to the RND pin. A random address is fixed based on the "H" level time of the RND pin during IC oscillation. Random address is captured at the fall of the RND pin, and voice playback commences. Therefore, when power is turned on, or when RESET is input, the phrase at fixed address "0001" is played while the random counter remains initialized until random playback is initiated.

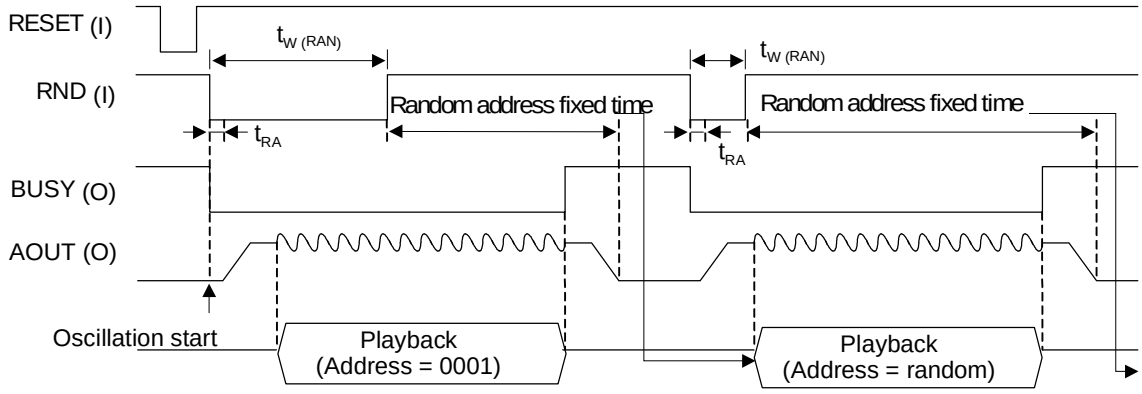


Figure 3.3 Random Address Capture

Table 3.2 Random Playback Address

A2, A1	A0, SW2 to SW0	Phrase (Sample)
00	0001	Hit
	0010	Hit
	0011	Hit
	0100	Out
	⏐	⏐
	1111	Out
01	0001	Hit
	0010	Out
	0011	Out
	0100	Out
	⏐	⏐
	1111	Out
10	0001	White
	0010	Black
	0011	Red
	0100	Blue
	⏐	⏐
	1111	Green
11	0001	
	⏐	
	1111	

For a random address, 15 phrases can be set for each logical condition of addresses A2 and A1 (i.e., “00”, “01”, “10”, and “11”).

In random playback, the four logic states (“000000”, “010000”, “100000” and “110000”) in user-specified phrases cannot be used. Take it into consideration when creating ROM data.

A random address is set by the “H” level time of the RND pin, so if the same pulse width is input by microcontroller, the random address fixed time becomes constant, and a random phrase may not be played under these conditions. The random address fixed time must be inconsistent in order to produce random playback.

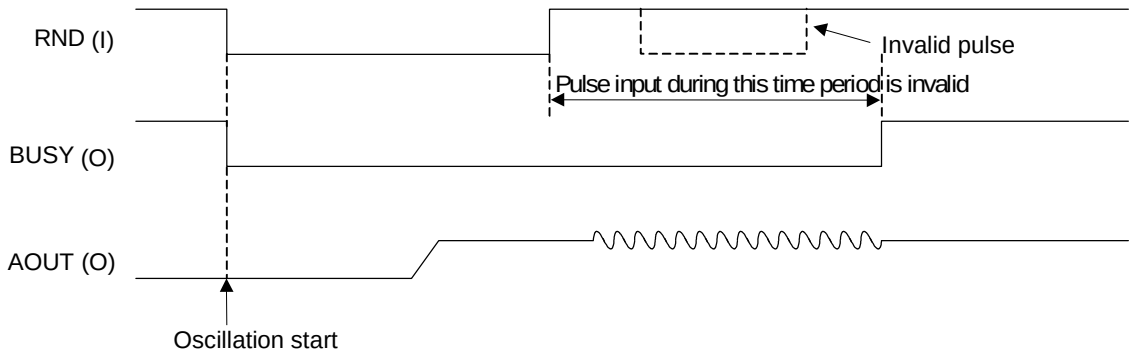


Figure 3.4 Timing when a Pulse is Input to the RND Pin During Random Playback

Table 3.3 Random Playback and Stop Address

A2, A1	A0, SW2-SW0 *	Code Details
00	0001 | 1111	Random playback address (15 addresses)
01	0001	Stop address

* Address(es) corresponding to the A0 and SW2-SW0 pins

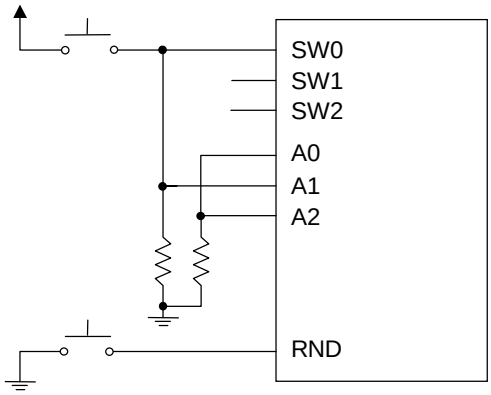
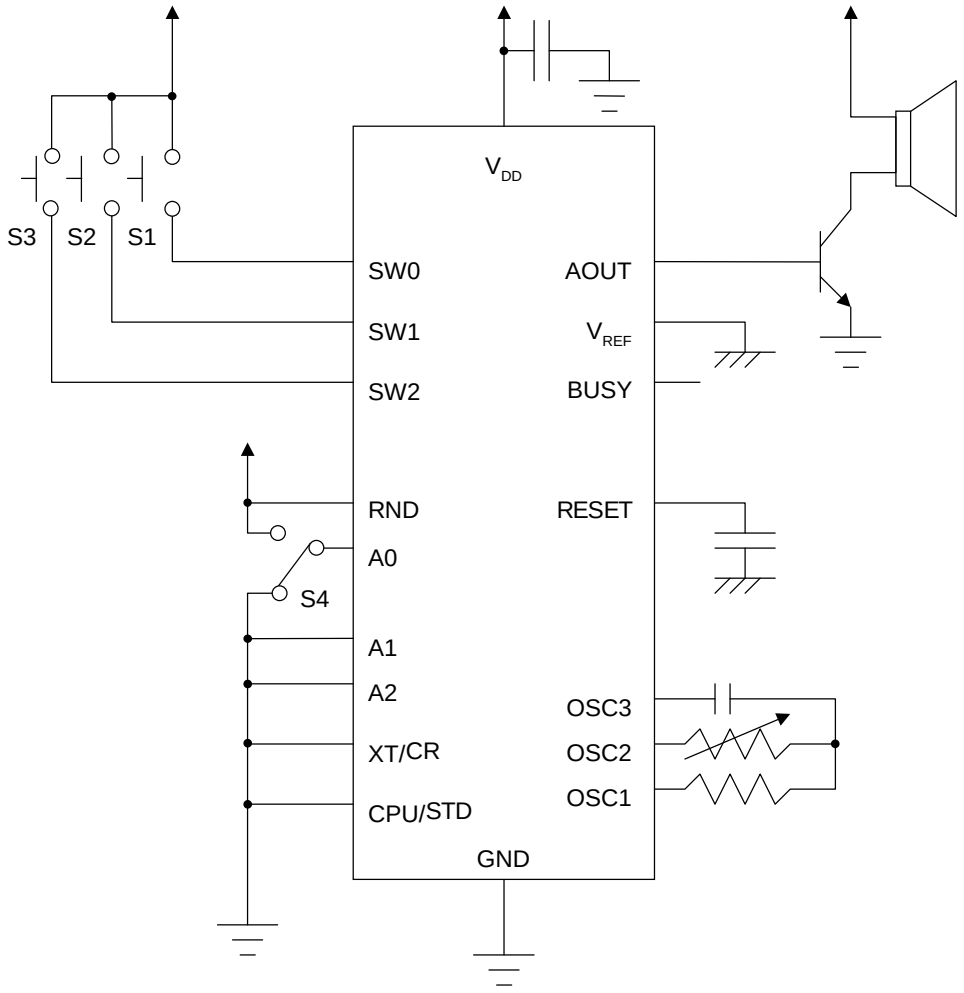


Figure 3.5 Circuit Example for Random Playback Stop

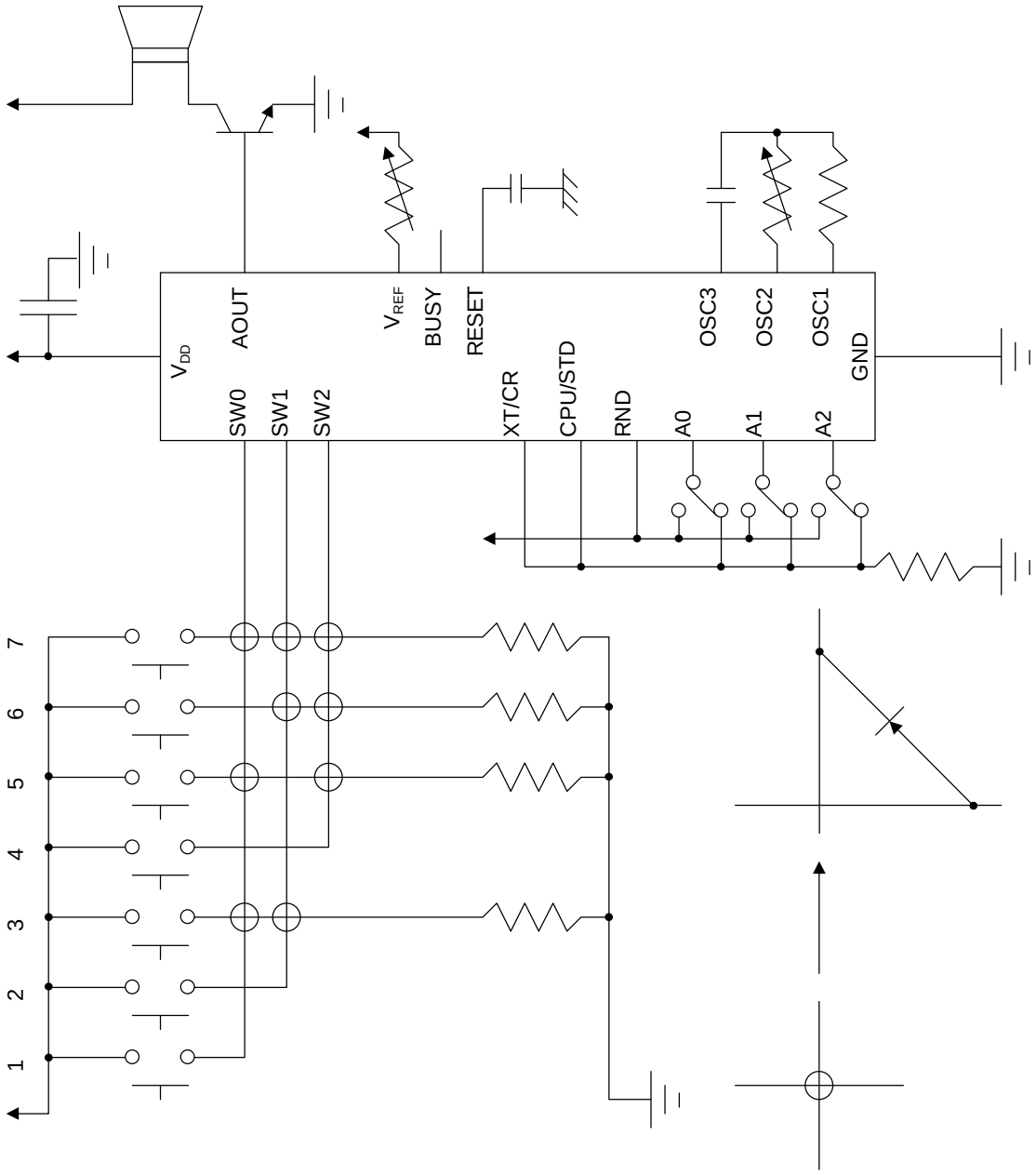
An unused user-specified address is used as a stop address, therefore the IC can enter standby without voice playback, as shown in Figure 3.2.

APPLICATION CIRCUITS



		A2	A1	A0	SW2	SW1	SW0	Address [HEX]
S4 = “L”	S1	0	0	0	0	0	1	01
	S2	0	0	0	0	1	0	02
	S3	0	0	0	1	0	0	04
S4 = “H”	S1	0	0	1	0	0	1	09
	S2	0	0	1	0	1	0	0A
	S3	0	0	1	1	0	0	0C

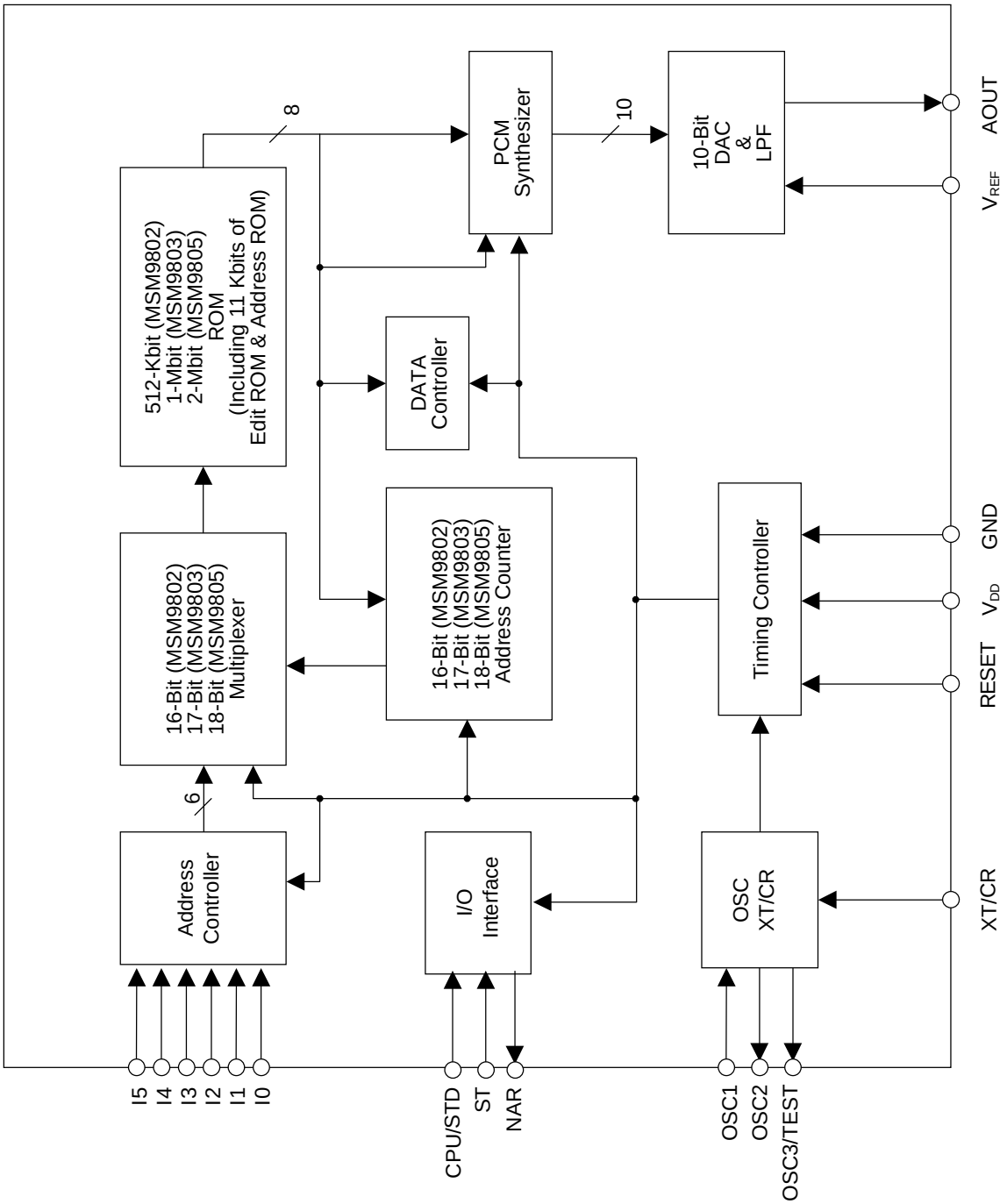
Application Circuit for Playing Six Phrases Using Four Switches



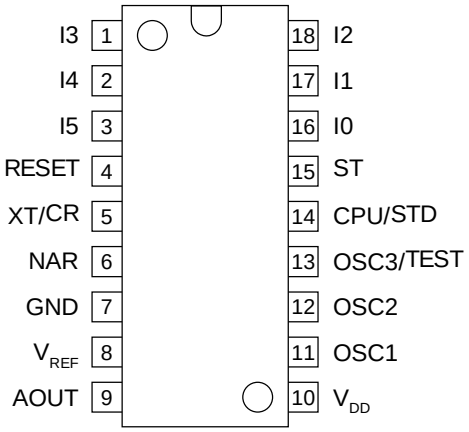
Application Circuit Using Switches

(2) MICROCONTROLLER INTERFACE MODE (CPU/STD: "H" LEVEL)

BLOCK DIAGRAM

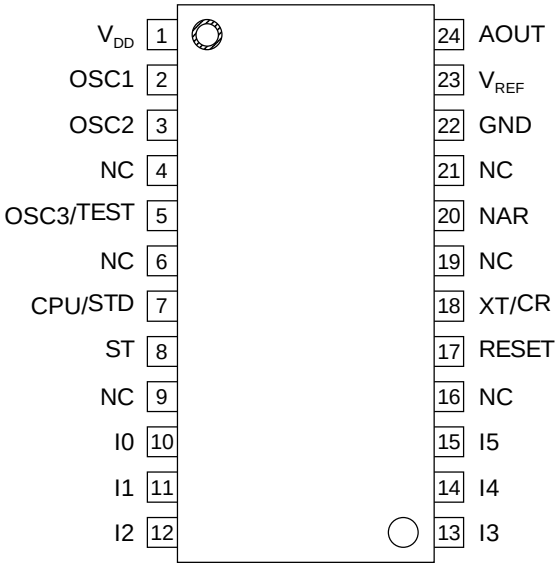


PIN CONFIGURATION (TOP VIEW)



18-Pin Plastic DIP

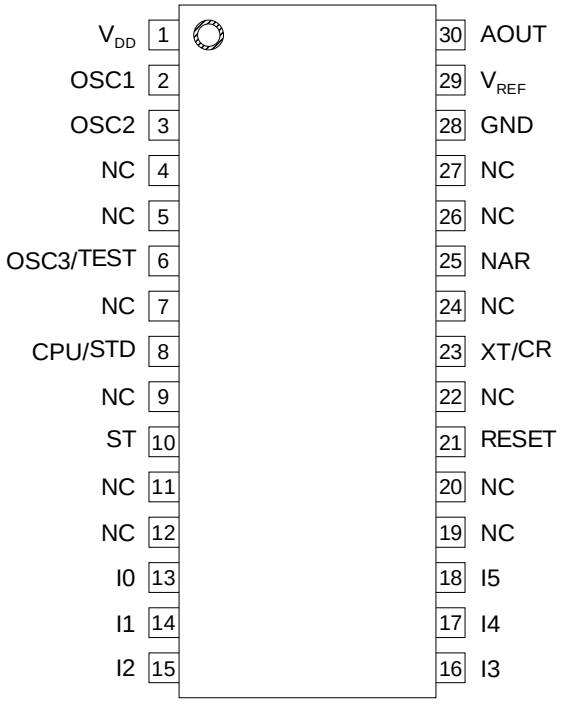
Note: Applicable to MSM9802-xxxRS, MSM9803-xxxRS, and MSM9805-xxxRS.



NC: No connection

24-Pin Plastic SOP

Note: Applicable to MSM9802-xxxGS-K, MSM9803-xxxGS-K, and MSM9805-xxxGS-K.



NC: No connection

30-Pin Plastic SSOP

Note: Applicable to MSM9802-xxxGS-AK, MSM9803-xxxGS-AK, and MSM9805-xxxGS-AK.

PIN DESCRIPTIONS

Pin			Symbol	Type	Description
DIP	SOP	SSOP			
4	17	21	RESET	I	The IC enters the standby state if this pin is set to "L" level. At this time, oscillation stops and AOUT drives a current of 0 mA and becomes GND level, then the IC returns to the initial state. Apply a "L" pulse upon power-on. This pin has an internal pull-up resistor.
6	20	25	NAR	O	Signal output pin that indicates whether the 6-bit LATCH (see Block Diagram) is idle. NAR at "H" level indicates that the LATCH is empty and ST input is enabled.
5	18	23	XT/CR	I	XT/CR switching pin. Set to "H" level if ceramic oscillation is used. Set to "L" level if CR oscillation is used.
14	7	8	CPU/STD	I	Microcontroller interface/stand-alone mode switching pin. Set to "H" level if the MSM9802/03/05 is used in microcontroller interface mode.
8	23	29	V_{REF}	I	Volume setting pin. If this pin is set to GND level, the maximum current is forced in, and if set to V_{DD} level, the minimum current is forced in. An approx. 10 kΩ pull-down resistor is internally connected to this pin during operation.
9	24	30	AOUT	O	Voice output pin. The voice signals are output as current changes. In standby state, this pin drives a current of 0 mA and becomes GND level.
7	22	28	GND	—	Ground pin.
10	1	1	V_{DD}	—	Power supply pin. Insert a bypass capacitor of 0.1 µF or more between this pin and the GND pin.
11	2	2	OSC1	I	Ceramic oscillator connection pin when ceramic oscillation is selected. CR connection pin when CR oscillation is selected. Input from this pin if external clock is used.
12	3	3	OSC2	O	Ceramic oscillator connection pin when ceramic oscillation is selected. CR connection pin when CR oscillation is selected. Leave this pin open if external clock is used. Outputs "L" level in standby state.
13	5	6	OSC3/TEST	O	Leave this pin open when ceramic oscillation is used. CR connection pin when CR oscillation is selected. Outputs "H" level in standby state when CR oscillation is selected.
15	8	10	ST	I	Voice synthesis starts at fall of ST, and addresses I0 to I5 are fetched at rise of ST. Input ST when NAR, the status signal, is at "H" level. This pin has internal pull-up resistor.
16-18 1-3	10-15	13-18	I0 - I5	I	Phrase input pins corresponding to playback sound.

ABSOLUTE MAXIMUM RATINGS

(GND = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +7.0	V
Input Voltage	V_{IN}		–0.3 to V_{DD}+0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND = 0V)

Parameter	Symbol	Condition	Rating			Unit
Power Supply Voltage	V_{DD}	—	2.0 to 5.5			V
Operating Temperature	T_{op}	—	–40 to +85			°C
Original Oscillation Frequency 1	f_{OSC1}	When crystal is selected	Min.	Typ.	Max.	MHz
			3.5	4.096	4.5	
Original Oscillation Frequency 2	f_{OSC2}	When CR is selected (*1)	200	256	300	kHz

*1 The accuracy of the oscillation frequency when CR oscillation is selected depends largely on the accuracy of the external R and C.

ELECTRICAL CHARACTERISTICS

DC Characteristics (1)

(V_{DD} = 5.0 V, GND = 0 V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	4.2	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.8	V
"H" Output Voltage	V_{OH}	I_{OH} = –1 mA	4.6	—	—	V
"L" Output Voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V
"H" Input Current 1	I_{IH1}	$V_{IH} = V_{DD}$	—	—	10	µA
"H" Input Current 2	I_{IH2}	Applies to OSC1 pin only. $V_{IH} = V_{DD}$	—	—	15	µA
"L" Input Current 1	I_{IL1}	V_{IL} = GND	–10	—	—	µA
"L" Input Current 2 *1	I_{IL2}	Internal pull-up resistor	–200	–90	–30	µA
Dynamic Supply Current 1 *2	I_{DD1}	$V_{REF} = V_{DD}$, AOUT bias voltage = 0V	—	0.4	1	mA
Dynamic Supply Current 2 *3	I_{DD2}	At maximum output current V_{REF} = GND, AOUT bias voltage = 0V	—	—	16	mA
Standby Current	I_{DS}	Ta = –40 to +70°C	—	—	10	µA
		Ta = 70 to 85°C	—	—	50	µA
AOUT Output Current	I_{AOUT}	At maximum output current, V_{REF} = GND, AOUT bias voltage = 0V	6	9.5	15	mA
V_{REF} Pin Pull-down Resistance	R_{VREF}	—	7	10	13	kΩ

*1 Applicable to RESET, ST

*2 Dynamic supply current (excluding DAC output current)

*3 Dynamic supply current at maximum output current

DC Characteristics (2)

(V_{DD} = 3.1 V, GND = 0 V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage	V_{IH}	—	2.7	—	—	V
"L" Input Voltage	V_{IL}	—	—	—	0.5	V
"H" Output Voltage	V_{OH}	I_{OH} = –1 mA	2.6	—	—	V
"L" Output Voltage	V_{OL}	I_{OL} = 2 mA	—	—	0.4	V
"H" Input Current 1	I_{IH1}	$V_{IH} = V_{DD}$	—	—	10	µA
"H" Input Current 2	I_{IH2}	Applies to OSC1 pin only. $V_{IH} = V_{DD}$	—	—	15	µA
"L" Input Current 1	I_{IL1}	V_{IL} = GND	–10	—	—	µA
"L" Input Current 2 *1	I_{IL2}	Internal pull-up resistor	–100	–30	–10	µA
Dynamic Supply Current 1 *2	I_{DD1}	$V_{REF} = V_{DD}$, AOUT bias voltage = 0V	—	0.15	0.5	mA
Dynamic Supply Current 2 *3	I_{DD2}	At maximum output current V_{REF} = GND, AOUT bias voltage = 0V	—	—	5.5	mA
Standby Current	I_{DS}	Ta = –40 to +70°C	—	—	5	µA
		Ta = 70 to 85°C	—	—	20	µA
AOUT Output Current	I_{AOUT}	At maximum output current, V_{REF} = GND, AOUT bias voltage = 0V	1.4	3.2	5	mA
V_{REF} Pin Pull-down Resistance	R_{VREF}	—	7	10	13	kΩ

*1 Applicable to RESET, ST

*2 Dynamic supply current (excluding DAC output current)

*3 Dynamic supply current at maximum output currents

AC Characteristics

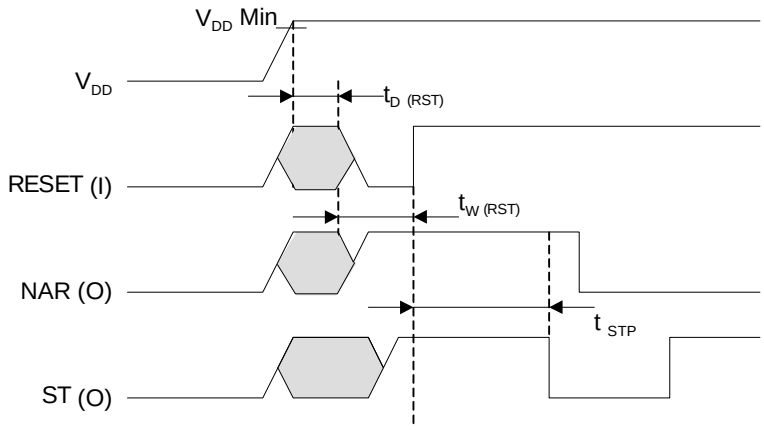
(V_{DD} = 5.0 V, GND = 0 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Master Clock Duty Cycle	f_{duty}	—	40	50	60	%
RESET Input Pulse Width	$t_{w(RST)}$	—	10	—	—	µs
RESET Input Time After Power-on	$t_{D(RST)}$	—	0	—	—	µs
ST Signal Setup Time	t_{STP}	At power-on	1	—	—	µs
ST Input Pulse Width	$t_{(ST)}$	—	0.35	—	2000	µs
ST-ST Pulse Interval	t_{SS}	Upon entering the stop code (note)	40	—	—	µs
Data Setup Time	t_{DW}	—	1	—	—	µs
Data Hold Time	t_{WD}	—	1	—	—	µs
NAR Output Time (1)	t_{SNS}	f_{SAM} = 8 kHz	—	—	10	µs
NAR Output Time (2)	t_{NAA}	f_{SAM} = 8 kHz (note)	350	375	400	µs
NAR Output Time (3)	t_{NAB}	f_{SAM} = 8 kHz (note)	315	440	500	µs
NAR Output Time (4)	t_{NAC}	f_{SAM} = 8 kHz (note)	350	375	500	µs
D/A Converter Change Time	t_{DAR}, t_{DAF}	— (note)	60	64	68	ms
Standby Transition Time (at end of voice output)	t_{STB}	— (note)	200	250	300	ms
Silence Time Between Phrases	t_{BLN}	f_{SAM} = 8 kHz (note)	350	375	500	µs

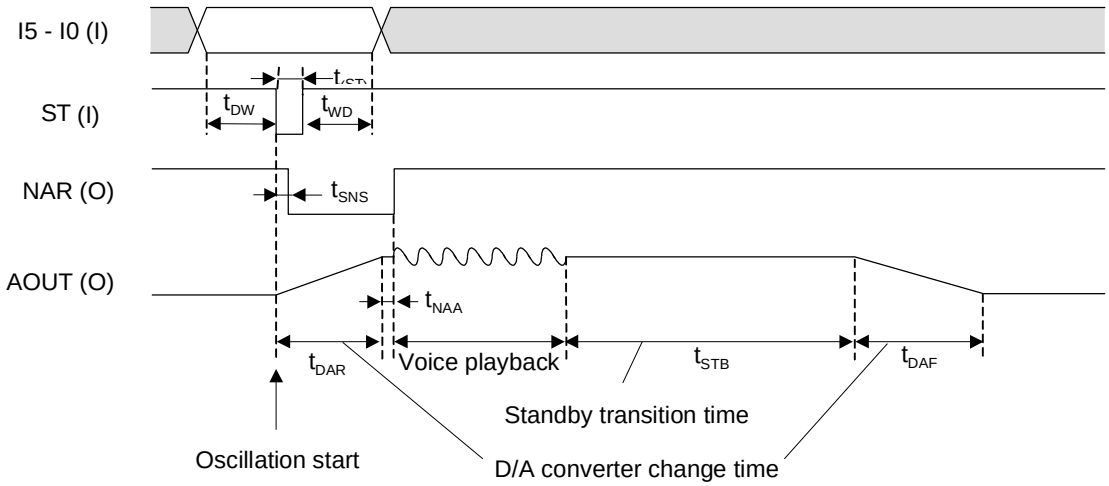
(Note) Proportional to master the periods of oscillation frequencies f_{OSC1} and f_{OSC2}.
The rated values show values when the standard master oscillation frequency is used.

TIMING DIAGRAMS

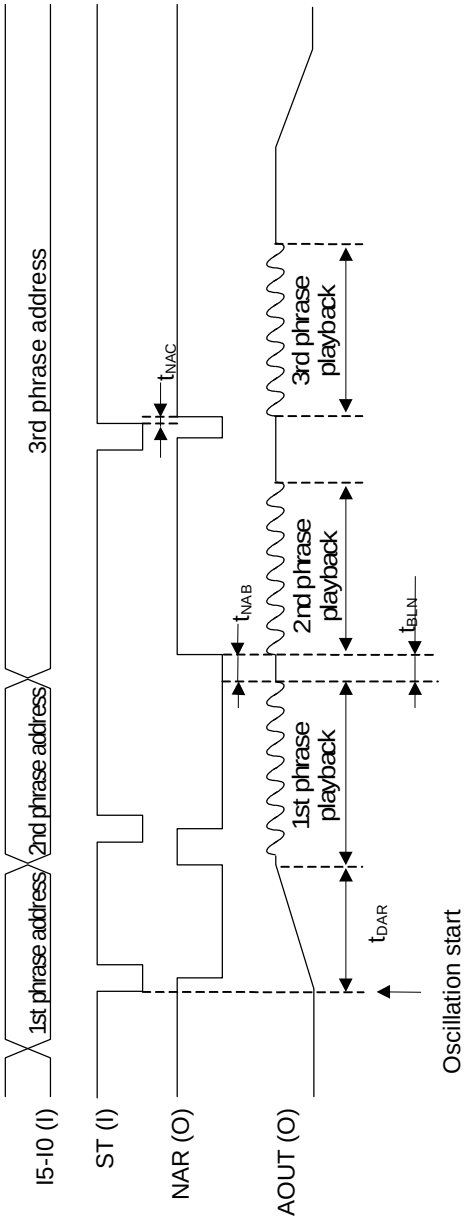
AC Characteristics at Power-On



AC Characteristics in Standby Status and when the IC is Activated



Playback Timing



FUNCTIONAL DESCRIPTION

1. Playback Code Specification

The user can specify a maximum of 63 phrases. Table 1.1 shows the settings by the I5-I0 pins.

Table 1.1 User-specified Phrases

I5-I0	Code Details
000000	Stop code
000001 | 111111	User-specified phrase (63 Phrases)

2. Address Data

If a phrase is input at I5-I0 pins by address data, and if a ST pulse is then applied, voice playback starts. Figure 2.1 shows voice start timing. Figure 2.2 shows timing when an address other than a phrase is input.

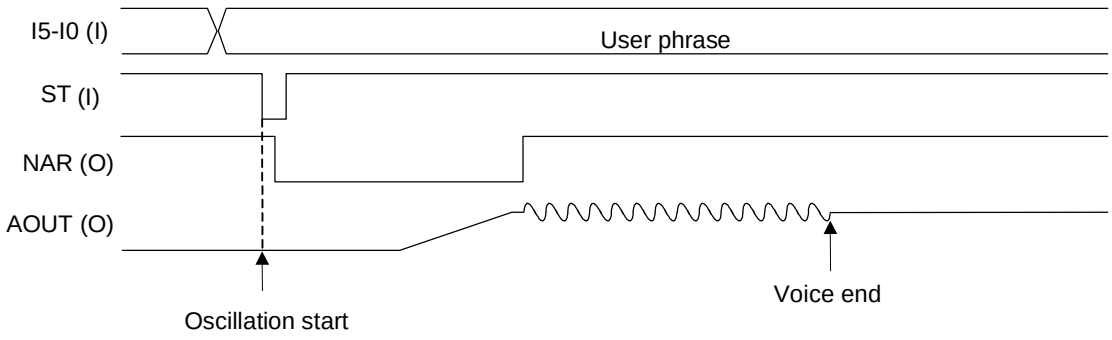


Figure 2.1 Voice Start Timing

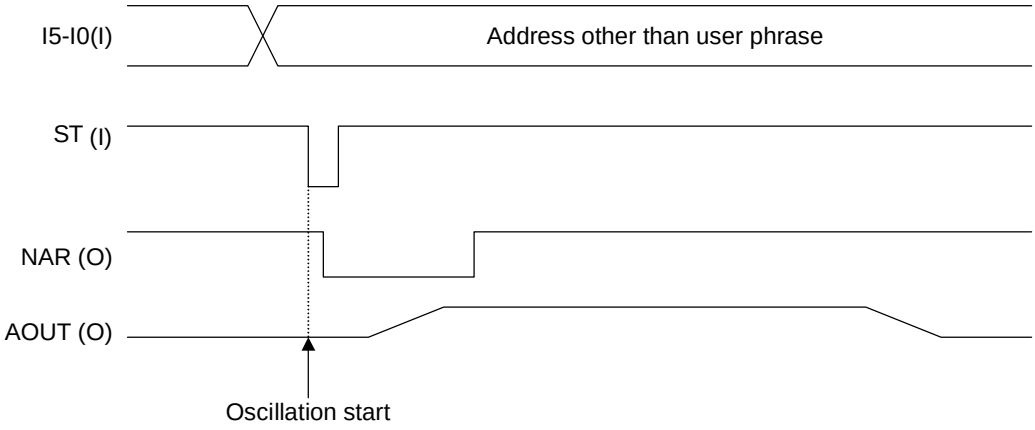


Figure 2.2 Timing when Address Other than a Phrase is Input in Stand-by Mode

3. Stop Code

If I5-I0 are set to "000000" during voice playback, and a ST signal is input, playback stops regardless of whether NAR is at "H" or "L" level, then AOUT becomes 1/2 I_{AOUT}. Stop code becomes valid at the falling edge of ST.

Figure 3.1 shows stop code input timing.

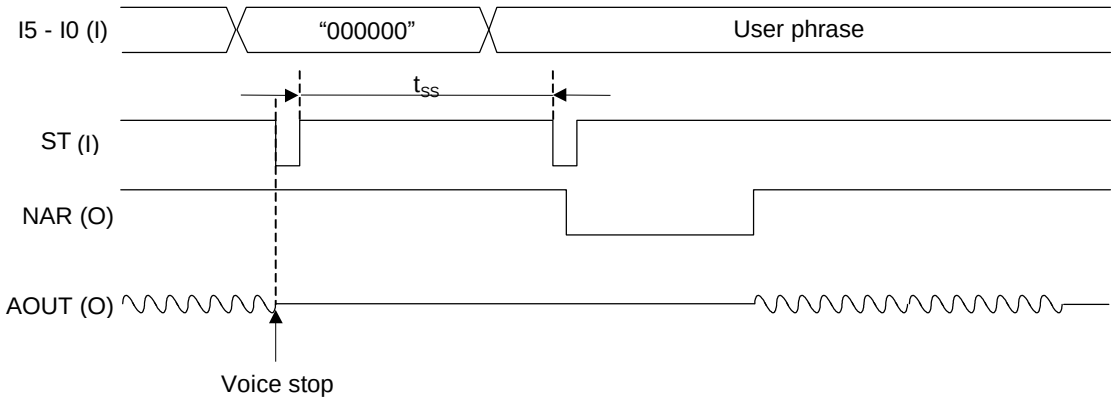


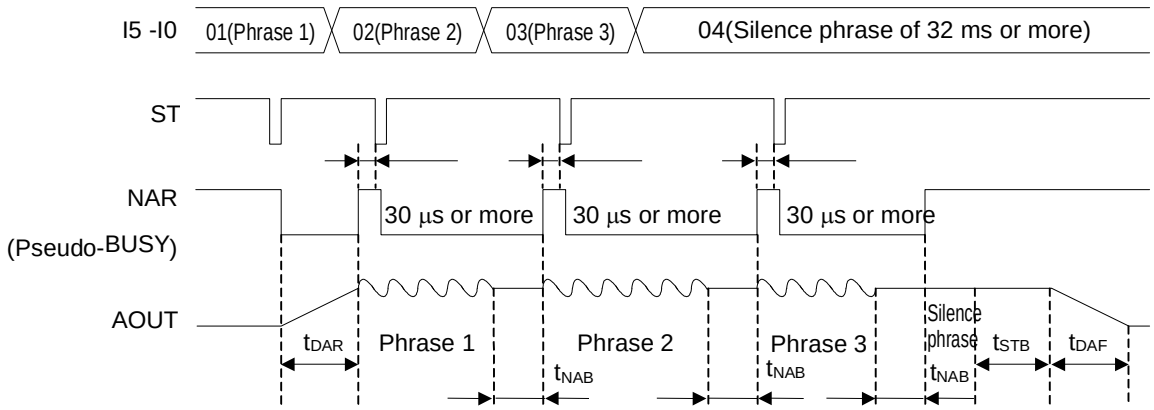
Figure 3.1 Stop Code Input Timing

The stop code does not initialize internal units but only stops playback. To initialize an internal register, use the RESET pin.

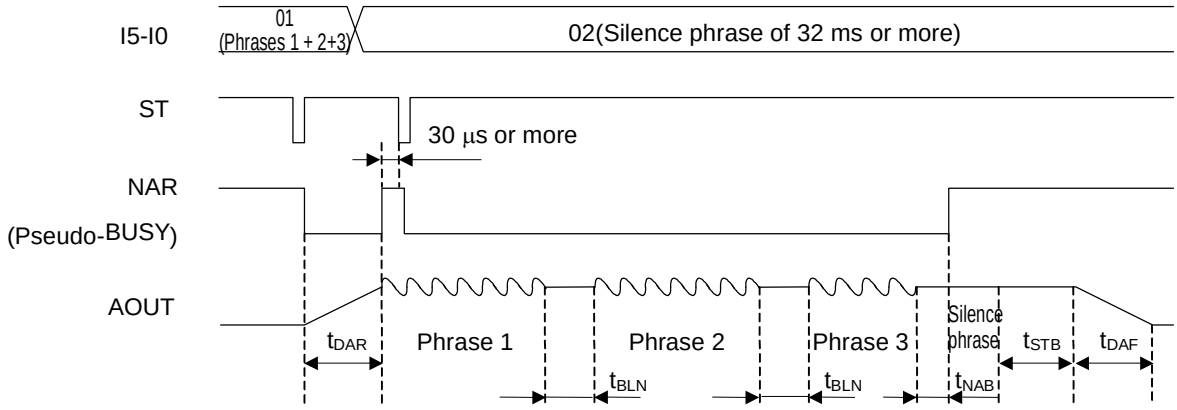
4. Generating Pseudo-BUSY Signal through NAR Pin

If the application in use requires a BUSY signal when this IC is used in microcontroller interface mode, a pseudo-BUSY signal can be generated through the NAR pin by controlling signal timing, as shown below.

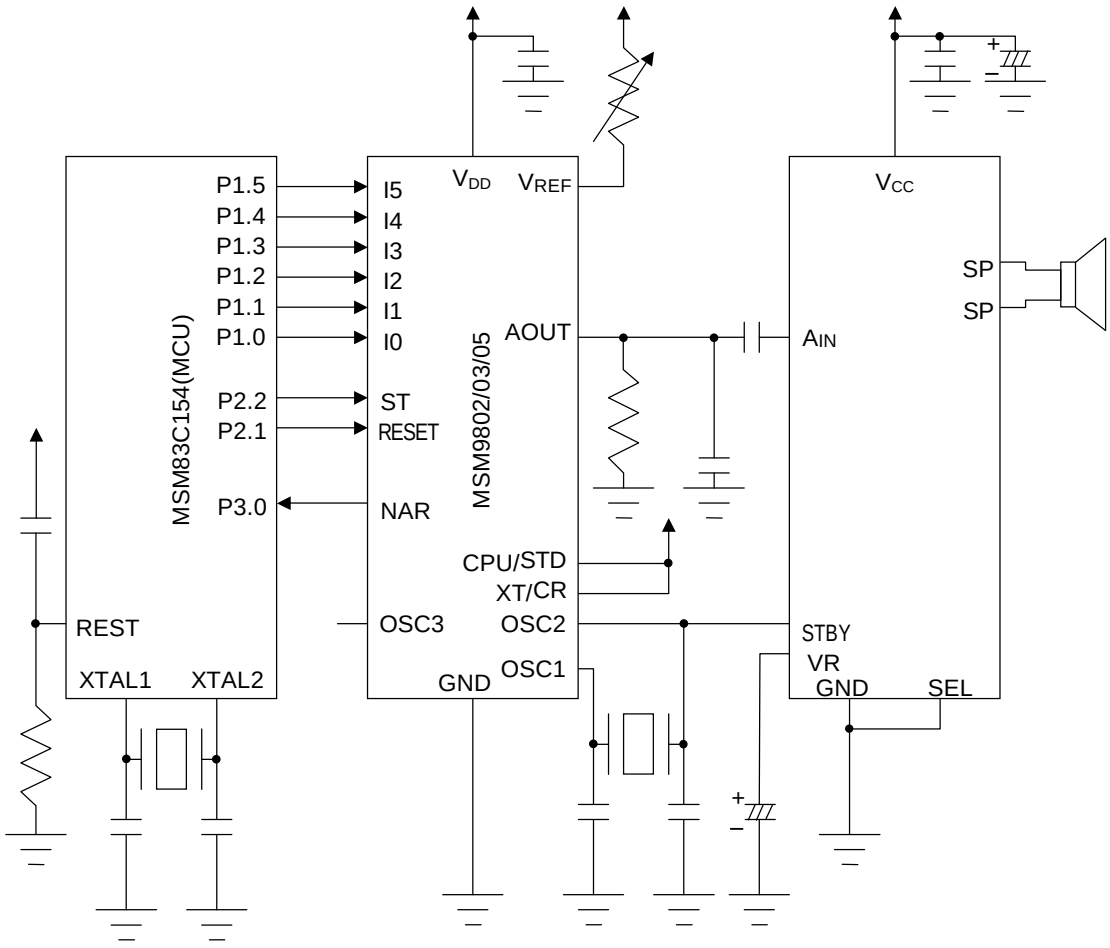
When edit ROM is not used



When edit ROM is used



APPLICATION CIRCUIT



Application Circuit in Microcontroller Interface

(3) COMMON

Sampling Frequency

As shown in Table 1.1, 7 sampling frequencies are available.
A sampling frequency can be selected and assigned to each phrase in ROM data.

Table 1.1 Sampling Frequency

Sampling Frequency (At standard oscillation frequency)	Frequency diving ratio	
	XT/CR = "H" Ceramic Oscillation	XT/CR = "L" CR Oscillation
4.0 kHz	f_{OSC1}/1024	f_{OSC2}/64
5.3 kHz	f_{OSC1}/768	f_{OSC2}/48
6.4 kHz	f_{OSC1}/640	f_{OSC2}/40
8.0 kHz	f_{OSC1}/512	f_{OSC2}/32
10.6 kHz	f_{OSC1}/384	Unavailable
12.8 kHz	f_{OSC1}/320	Unavailable
16.0 kHz	f_{OSC1}/256	Unavailable

Note: When CR oscillation is selected, 10.6 kHz, 12.8 kHz, and 16 kHz cannot be selected.

Recording/Playback Time

Figure 2.1 below shows memory allocation of the on-chip Mask ROM. About 11 Kbits of data area is allocated for the Phrase Control Table, Phrase Data Control and Test Data.
Therefore, actual data area for storing sound data equals the total Mask ROM capacity minus 11 Kbits.

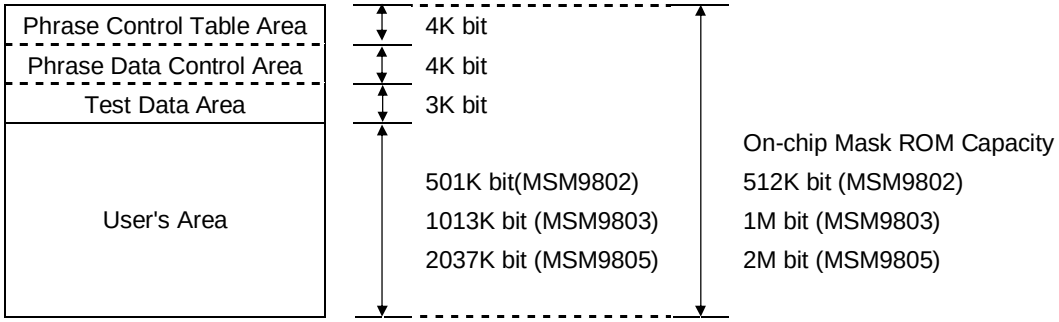


Figure 2.1 Memory Allocation of On-chip Mask ROM

The playback time is obtained by dividing the memory capacity by the bit rate.
The playback time for 8-bit PCM algorithm is obtained by using the following equation.

$$\text{Playback time [sec]} = \frac{\text{Memory capacity [bit]}}{\text{Bit rate [bps]}} = \frac{\text{Memory capacity [bit]}}{\text{Sampling frequency [Hz]} \times 8 \text{ [bit]}}$$

For example, if all phrases are stored in the MSM9802 at 8 kHz sampling frequency, the maximum playback time is as follows.

$$\text{Playback time} = \frac{(512-11) \times 1024 \text{ [bit]}}{8000 \text{ [Hz]} \times 8 \text{ [bit]}} \cong 8.0 \text{ [sec]}$$

Table 2.1 Maximum playback time

Model	ROM capacity	User's area	Maximum playback time (sec)			
			f_{SAM} = 4.0 kHz	f_{SAM} = 6.4 kHz	f_{SAM} = 8.0 kHz	f_{SAM} = 16.0 kHz
MSM9802	512K bit	501K bit	16.0	10.0	8.0	4.0
MSM9803	1M bit	1013K bit	32.4	20.2	16.2	8.1
MSM9805	2M bit	2037K bit	65.1	40.7	32.5	16.2

Playback Method

This IC provides two kinds of playback methods, non-linear PCM algorithm and straight PCM algorithm. When the 8-bit non-linear PCM algorithm is selected, sound quality can be improved because a resolution equivalent to 10-bit straight PCM is available around the waveform center. You can select either non-linear PCM algorithm or straight PCM algorithm for each phrase. Table 3.1 shows the relationship between playback methods and applicable sounds. It is recommended to evaluate the sound quality before actual use.

Table 3.1 Relationship between playback methods and applicable sounds

Playback method	Applicable sound
8-bit non-linear PCM algorithm	Human voice
8-bit straight PCM algorithm	BEEP tone, sound effects

Phrase Control Table

Because the LSI contains the Phrase Control Table, it is possible to play back multiple phrases in succession by a single easy control operation like controlling a single regular phrase playback. Up to 8 combined phrases including a silence can be registered in a single address in the Phrase Control Table.
Further, you can use the maximum memory space for data storage because it is not required to have the same phrase data.
To show an example, let's assume that your application needs to speak two similar sentences, "It is fine today" and "It is rainy today." The two sentences have the common words "it", "is" and "today". What you have to do is to prepare these common sound data, not in sentences but in words, and to store each combined phrase data in Phrase Control Table as shown in Table 4.1 and Figure 4.1
Multiple phrases can be played continuously merely by specifying a desired phrase using an X address. For an example from Table 4.1, when address "01" is specified, "It is fine today" is played, and when address"02" is specified, "It is rainy" is played.
Phrase Control Table, a silence can be inserted without using the User's Area.

Minimum time for silence	32 ms
Maximum time for silence	2016 ms
Time unit for setting up silence	32 ms

Table 4.1 Matrix of the Phrase Control Table

No.	X-Address (HEX)	Y-Address (Up to 8 phrases)								Sound Data
1	01	[01]	[02]	Silence	[10]	[03]				It is (silence) fine today.
2	02	[01]	[02]	Silence	[12]	[03]				It is (silence) rainy today.
3	03	[01]	[02]	[10]	[21]	[11]	[12]	[22]	[03]	It is fine becoming cloudy, rainy in some areas today.
62	3E									
63	3F									

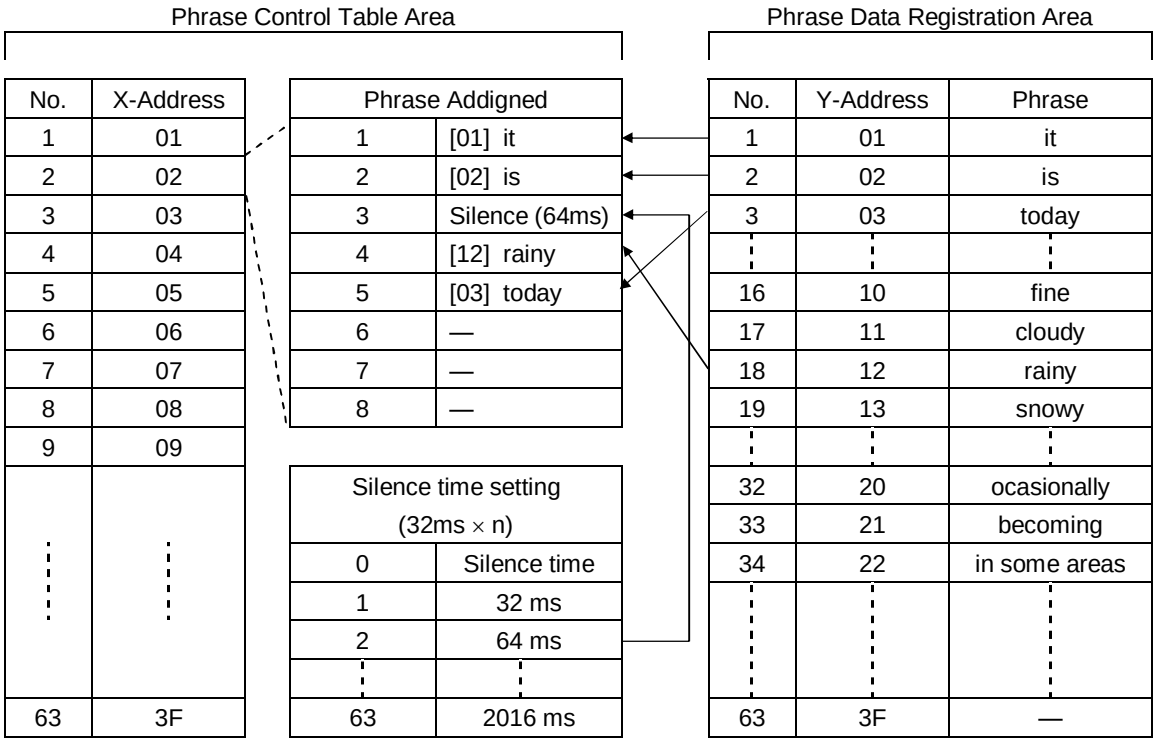


Figure 4.1 Phrase Combination Matrix for Phrase Control Table

CR Oscillation

Figure 5.1 shows an external circuit using CR oscillation. Figure 5.2 shows the CR oscillation frequency characteristics.

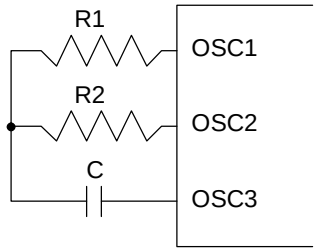


Figure 5.1 CR Oscillation

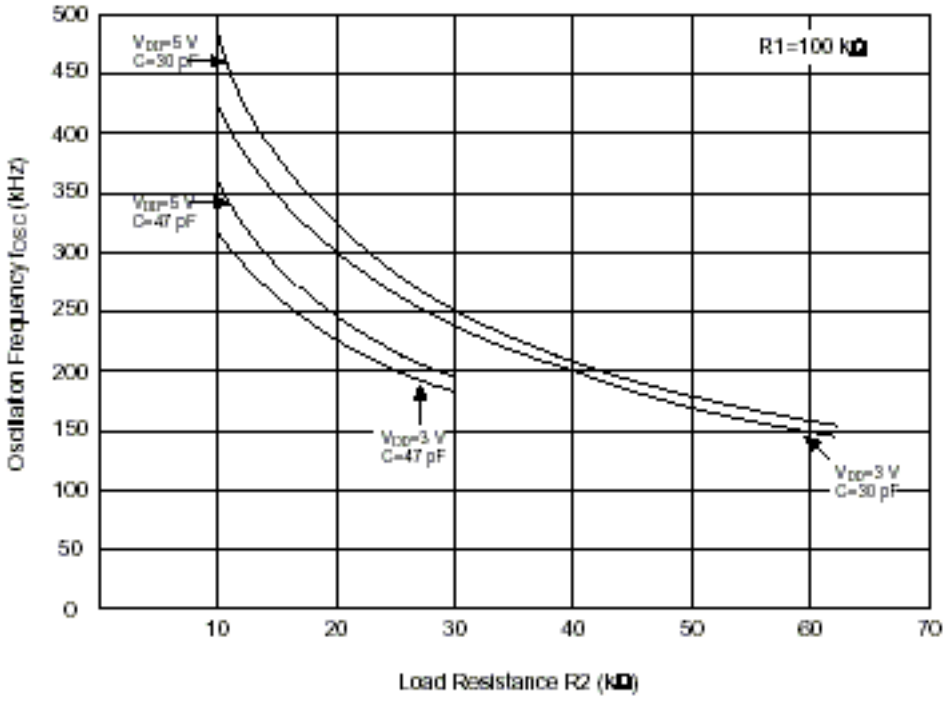


Figure 5.2 CR Oscillation Frequency Characteristics

Determining CR constants

The CR oscillation frequency characteristics are shown in Figure 5.2. If f_{osc} is set to 256 kHz, use the following values as a guide (see Figure 5.2) to set the C and R2 that fit the printed-circuit board type used.

R1 = 100 kΩ, R2 = 30 kΩ, C = 30 pF

When choosing CR oscillation, the CR oscillation frequency varies according to the fluctuation of the external C and R2.

Fluctuation of CR oscillation frequencies

When choosing CR oscillation, the error of CR oscillation frequency due to process variations of the IC is ± 4% maximum, and the fluctuation of the CR oscillation frequency when using a capacitor (C) of ± 1% accuracy and a resistor (R2) of ± 2% accuracy is a maximum of ± 7% approximately.

Ceramic Oscillation

Figure 6.1 shows an external circuit using a ceramic oscillator.

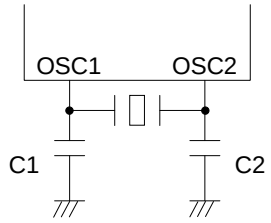


Figure 6.1 Ceramic Oscillation Diagram

For example, the following table shows the optimum load capacitances, power supply voltage ranges, and operating temperature ranges when ceramic oscillators made by Murata MFG Co., Ltd., Kyocera Co., Ltd. and TDK Co., Ltd. are used.

Ceramic oscillator			Optimal load capacity		Supply voltage range (V)	Operating temperature range (°C)
Maker	Type	Frequency (MHz)	C1 (pF)	C2 (pF)		
Murata MFG	CSTCR4M09G53-R0	4.096	Built in	Built in	2.3 to 5.5	–40 to +85
	CSTLS4M09G53-B0				2.4 to 5.5	
Kyocera	PBRC4.00A	4.0	33	33	3.1 to 5.5	–20 to +80
	KBR-4.0MSB					
	PBRC4.00B		Built in	Built in		
	KBR-4.0MKC					
TDK	CCR4.00MC3	4.0	Built in	Built in	2.4 to 5.5	–40 to +85

(Note) When a 4 MHz ceramic oscillator is used, the playback speed of MSM9802/03/05 is slower by 2 percent than that of an analysis tool or a demonstration board.

Low-Pass Filter

In this IC, all voice outputs are through the built-in low-pass filter (LPF). Figure 7.1 and Table 7.2 show the LPF frequency characteristics and LPF cutoff frequency respectively.
Only the voice output through LPF is enabled in this IC.

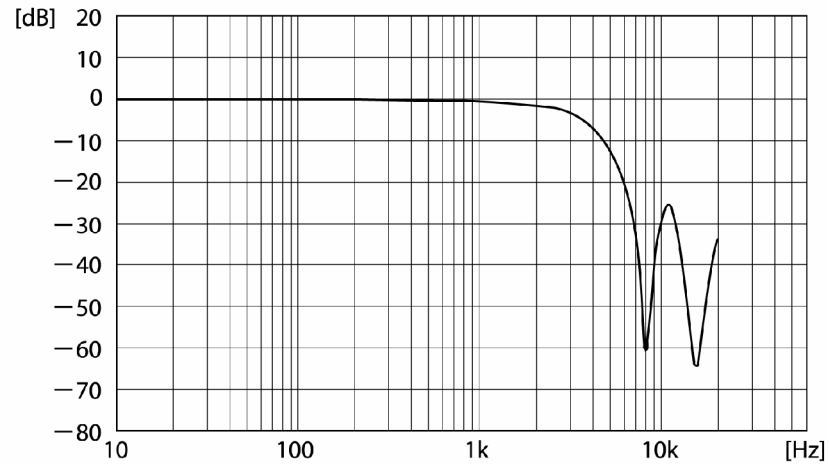


Figure. 7.1 LPF Frequency Characteristics (f_{SAM} = 8 kHz)

Table 7.2 LPF Cutoff Frequency

Sampling Frequency (kHz) (f_{SAM})	Cutoff Frequency (kHz) (f_{CUT})
4.0	1.2
5.3	1.6
6.4	2.0
8.0	2.5
10.6	3.2
12.8	4.0
16.0	5.0

Standby Transition

When playback of a phrase is finished, if playback of the next phrase does not start up within t_{STB} (0.25 sec. typ.), the IC enters standby status and the entire operation stops.

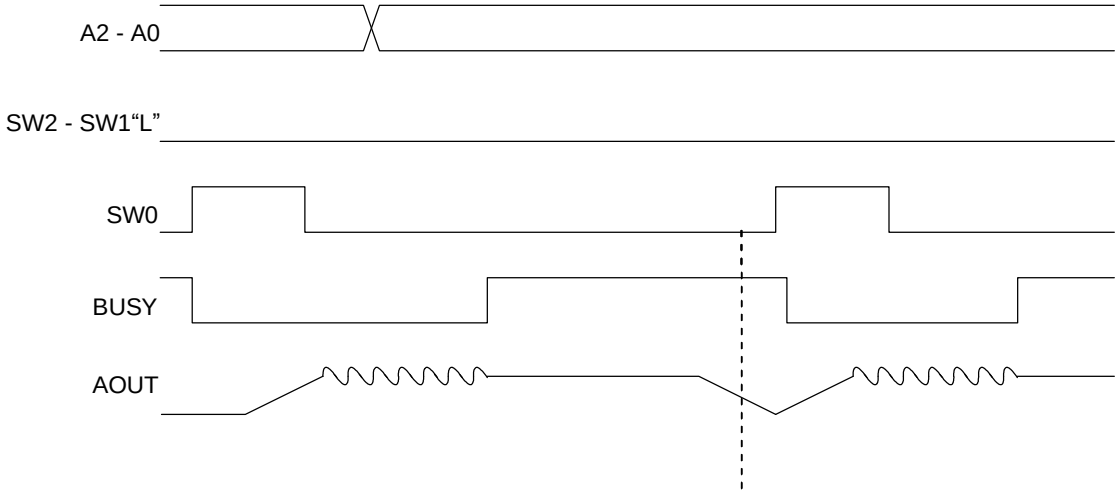


Figure 8.1 Timing for Voice Playback during D/A Converter Change Time (Stand-alone Mode)

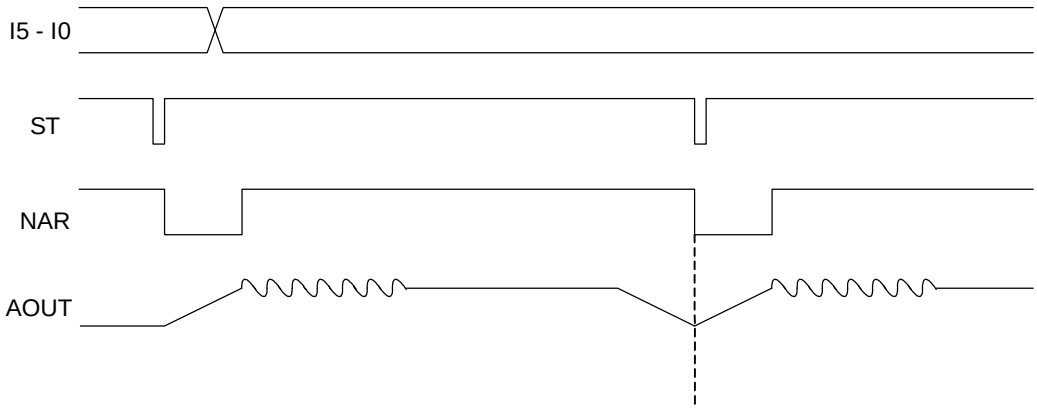
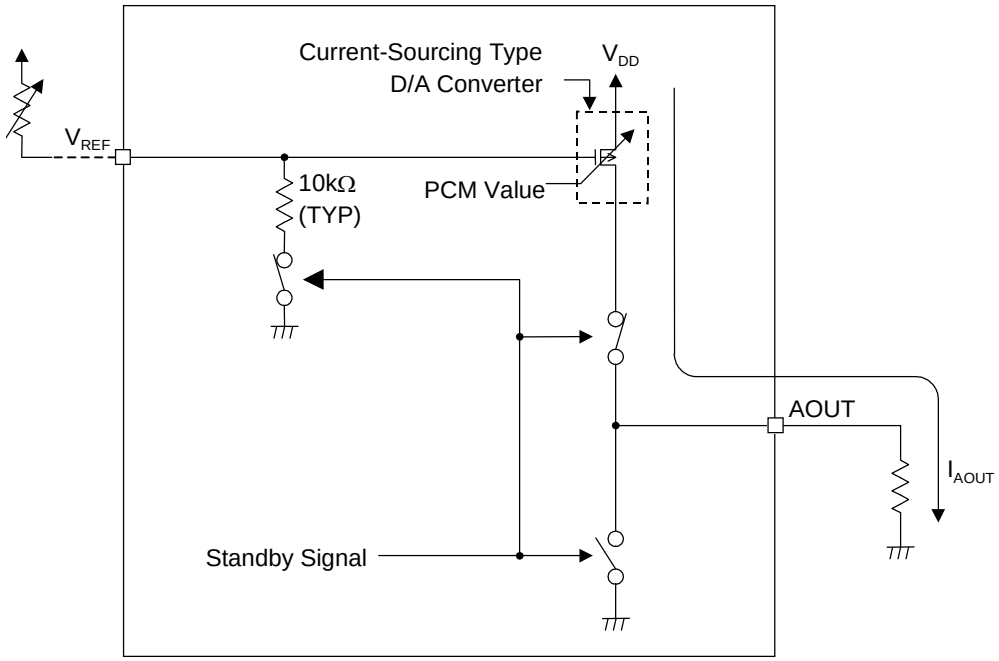


Figure 8.2 Timing for Voice Playback during D/A Converter Change Time (Microcontroller Interface Mode)

If playback is attempted during D/A converter change time as shown in figures 8.1 and 8.2, the IC exits from standby status and the output from the D/A converter begins going to the 1/2 I_{AOUT} level. When the output reaches 1/2 I_{AOUT}, voice playback starts.

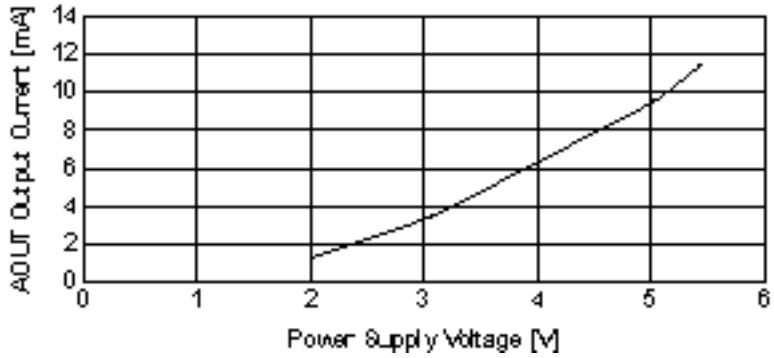
Voice Output Unit Equivalent Circuit (AOUT, FREF Pins)



(The above switch positions show those when the circuit is active.)

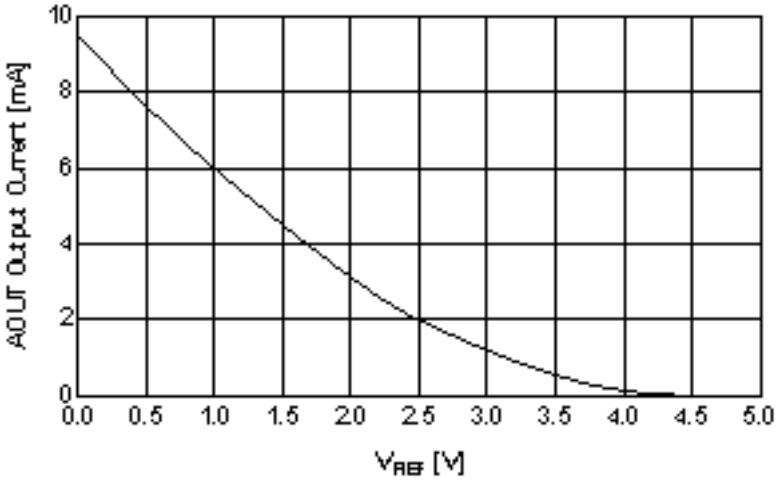
Figure 9.1 Voice Output Unit Equivalent Circuit

D/A CONVERTER OUTPUT CURRENT CHARACTERISTICS

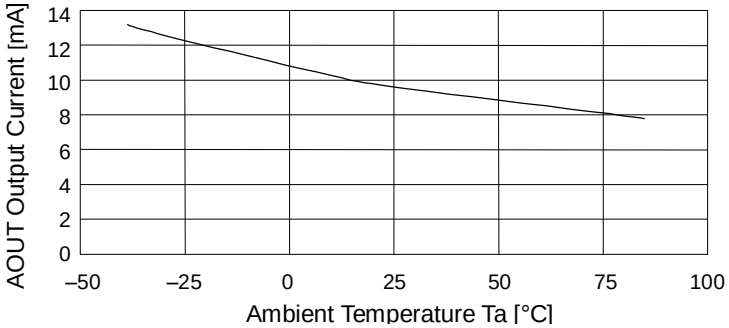


Power Supply Voltage vs. Output Current Characteristics (Ta = 25°C, V_{AOUT} = 0V)

Temperature vs. Output Current Characteristics (V_{DD} = 5V, V_{AOUT} = 0V)



V_{REF} Voltage vs. Output Current Characteristics (Ta = 25°C, V_{DD} = 5V, V_{AOUT} = 0V)

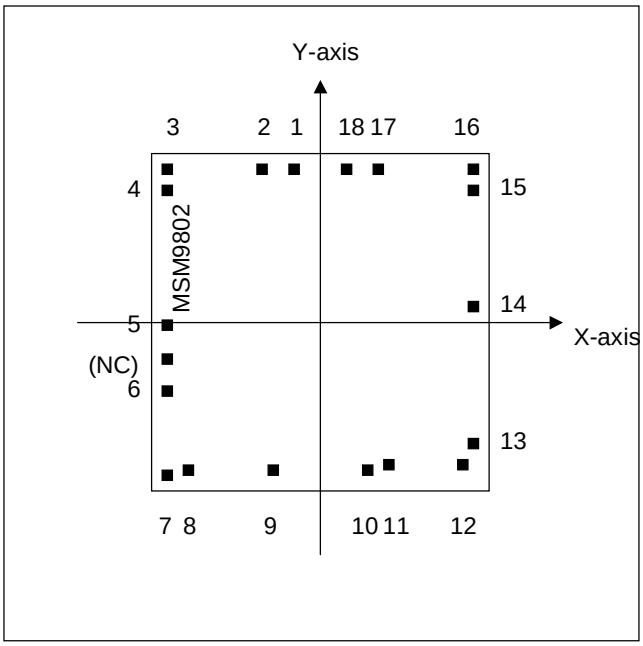


PAD CONFIGURATION

MSM9802

Pad Layout

Chip size : X = 3.22mm Y = 3.17mm
Chip thickness : 350 µm ± 30 µm
Pad size : 110 µm × 110 µm
Substrate potential : GND



Pad Coordinates

(Chip center is located at X = 0 and Y = 0)

(Unit: µm)

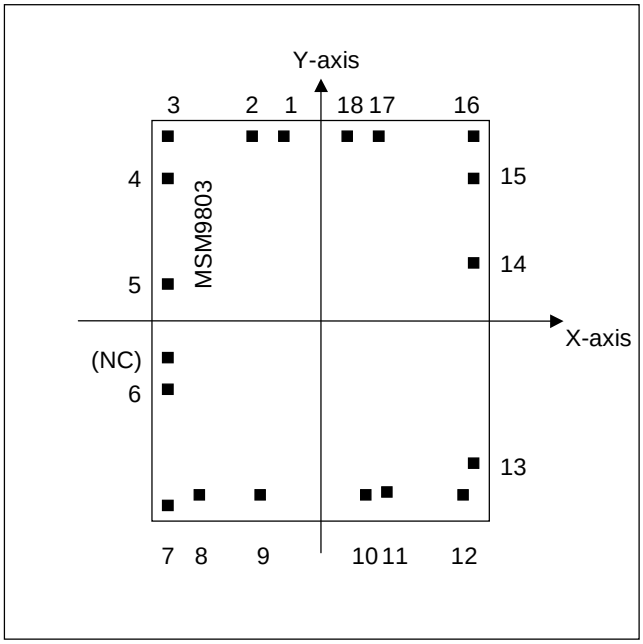
Pad No.	Pad Name	X-axis	Y-axis	Pad No.	Pad Name	X-axis	Y-axis
1	I3/ (A0)	–415	1385	10	VDD	462	–1347
2	I4/ (A1)	–816	1385	11	OSC1	742	–1333
3	I5/ (A2)	–1460	1385	12	OSC2	1349	–1333
4	RESET	–1460	1049	13	OSC3	1460	–972
5	XT/CR	–1458	–20	14	CPU/STD	1389	183
6	NAR	–1460	–899	15	ST/(RND)	1389	1058
7	GND	–1460	–1375	16	I0/(SW0)	1389	1385
8	V_{REF}	–1135	–1333	17	I1/(SW1)	719	1385
9	AOUT	–585	–1333	18	I2/(SW2)	276	1385

Pad name in parentheses is for stand-alone mode.

MSM9803

Pad Layout

Chip size : X = 3.22mm Y = 4.06mm
Chip thickness : 350µm ± 30µm
Pad size : 110µm × 110µm
Substrate potential : GND



Pad Coordinates

(Chip center is located at X = 0 and Y = 0)

(Unit: µm)

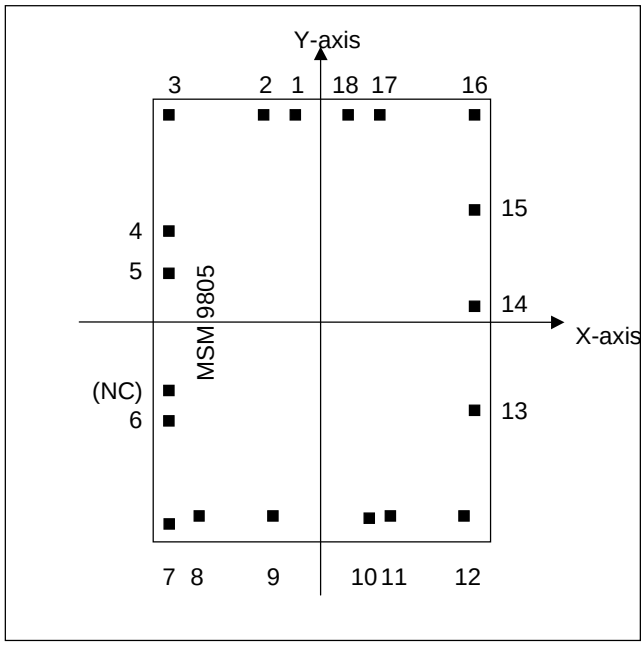
Pad No.	Pad Name	X-axis	Y-axis	Pad No.	Pad Name	X-axis	Y-axis
1	I3/ (A0)	–415	1829	10	VDD	452	–1788
2	I4/ (A1)	–816	1829	11	OSC1	742	–1776
3	I5/ (A2)	–1460	1829	12	OSC2	1349	–1776
4	RESET	–1460	1493	13	OSC3	1460	–1415
5	XT/CR	–1458	424	14	CPU/STD	1389	628
6	NAR	–1460	–1342	15	ST/(RND)	1389	1502
7	GND	–1460	–1818	16	I0/(SW0)	1389	1829
8	V_{REF}	–1135	–1776	17	I1/(SW1)	720	1829
9	AOUT	–585	–1776	18	I2/(SW2)	276	1829

Pad name in parentheses is for stand-alone mode.

MSM9805

Pad Layout

Chip size : X = 3.22mm Y = 5.96mm
Chip thickness : 350µm ± 30µm
Pad size : 110µm × 110µm
Substrate potential : GND



Pad Coordinates

(Chip center is located at X = 0 and Y = 0)

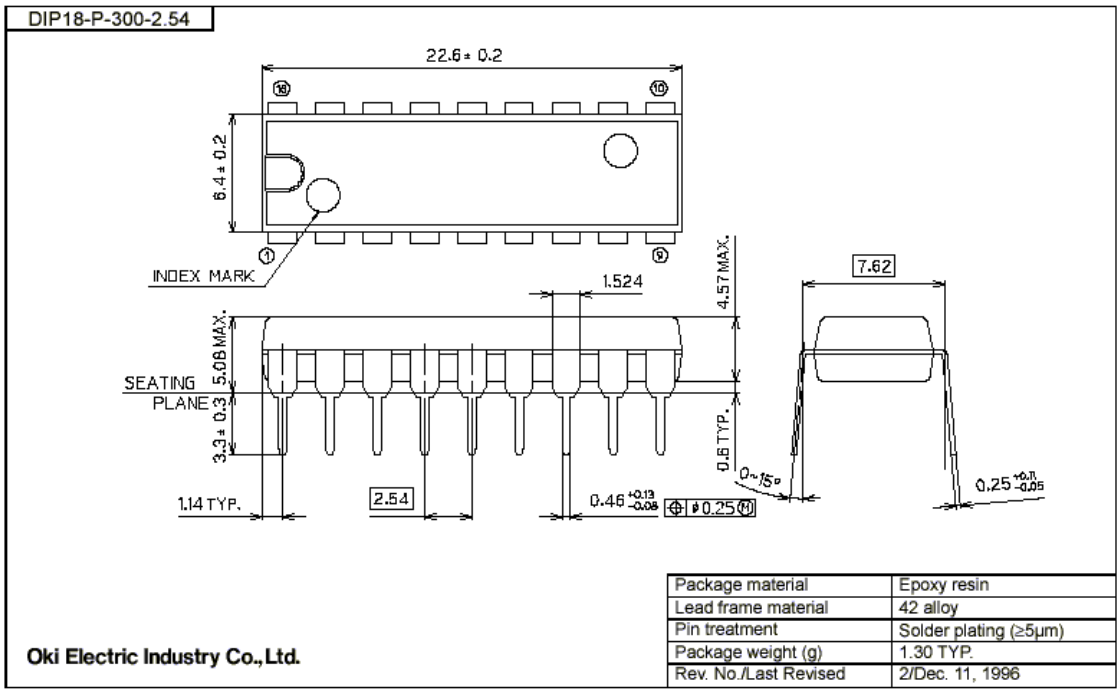
(Unit: µm)

Pad No.	Pad Name	X-axis	Y-axis	Pad No.	Pad Name	X-axis	Y-axis
1	I3/ (A0)	–415	2777	10	VDD	452	–2723
2	I4/ (A1)	–816	2777	11	OSC	742	–2726
3	I5/ (A2)	–1460	2777	12	OSC2	1349	–2726
4	RESET	–1460	882	13	OSC3	1460	–1532
5	XT/CR	–1458	364	14	CPU/STD	1453	267
6	NAR	–1460	–1546	15	ST/(RND)	1455	1338
7	GND	–1460	–2768	16	I0/(SW0)	1432	2777
8	VREF	–1136	–2726	17	I1/(SW1)	754	2777
9	AOUT	–585	–2726	18	I2/(SW2)	312	2777

Pad name in parentheses is for stand-alone mode.

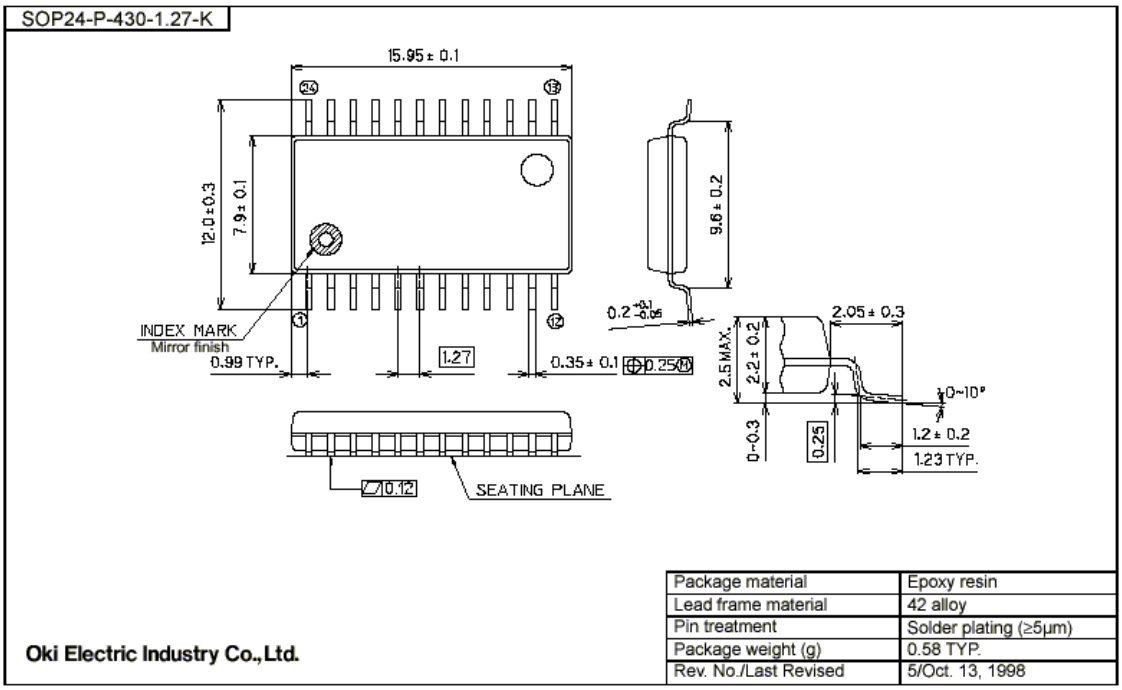
PACKAGE DIMENSIONS

(Unit: mm)



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	1.30 TYP.
Rev. No./Last Revised	2/Dec. 11, 1996

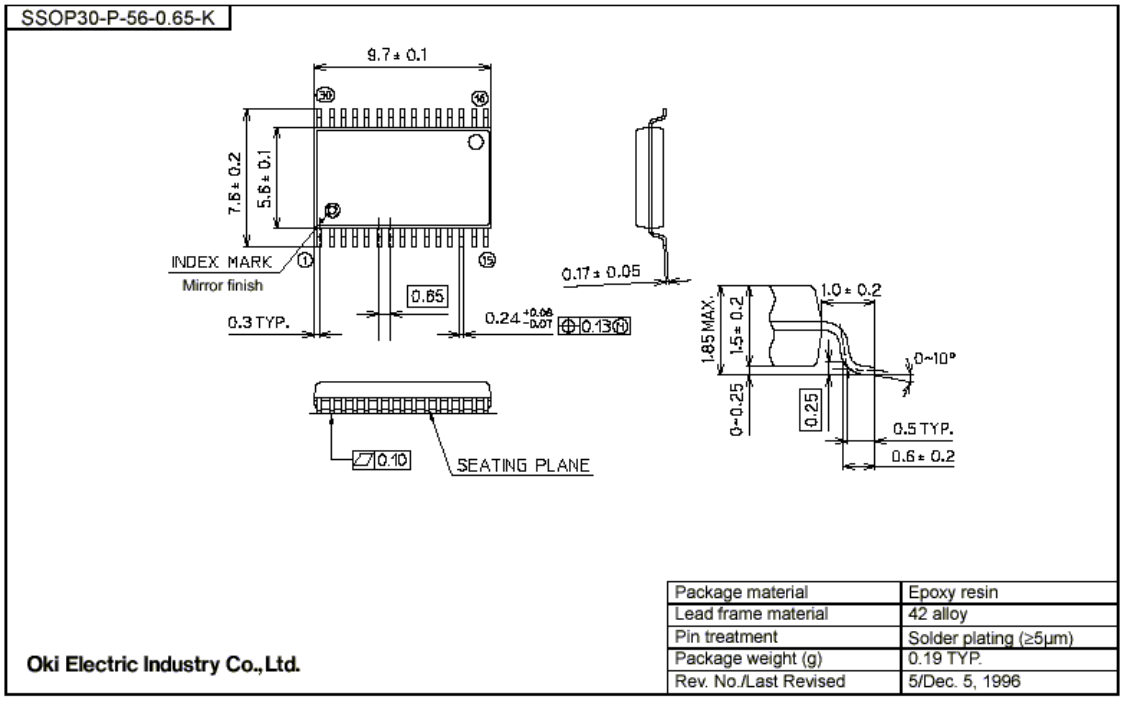
(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit: mm)



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5μm)
Package weight (g)	0.19 TYP.
Rev. No./Last Revised	5/Dec. 5, 1996

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL9802-03-05-04	Nov. 2001	–	–	Final edition 4
FEDL9802-03-05-05	Nov. 4, 2003	33	33	The pulse widths of the pseudo BUSY signals (through the NAR Pin) when edit ROM is not used and when edit ROM is used have been changed from 30 ms or more to 30 μs or more.
FEDL9802-03-05-06	Nov. 22, 2005	34	34	The AMP name was deleted in application circuit.

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