ML2011 DATASHEET

Version 3
Reviced on 20 November 2007

Contents

General Description

ML2011 is a high quality, low power consumption and small package MP3 decoder LSI which is base on hardware decoder solutions. It is suitable for the mobile phones and MP3 playback application in digital devices.

Features

1) On-chip hardwared MP3 decoder

2) Support MPEG-1/2/2.5 Layer3 Support MPEG-1/2/2.5 audio layer 3

3) Support Mono, Stereo mode

4) Support following bit rates
   MPEG-1 32/40/48/56/64/80/96/112/128/160/192/224/256/320
   MPEG-2/2.5 8/16/24/32/40/48/56/64/80/96/112/128/144/160

5) 3 or 4-pin serial interface or 8bit bus interface selectable

6) On-chip 2,048 bytes FIFO buffer memory

7) Built in DAC and Speaker Amplifier

8) Low power consumption at power-down: Idds = 2uA (TYP)
   Operating current: IDDD=45mA(MAX)

9) Power Supply:
   DVDD: +2.7 V ~ 3.6 V
   IOVDD: +1.65 V ~ DVDD
   SPVDD: DVDD ~ 4.5V

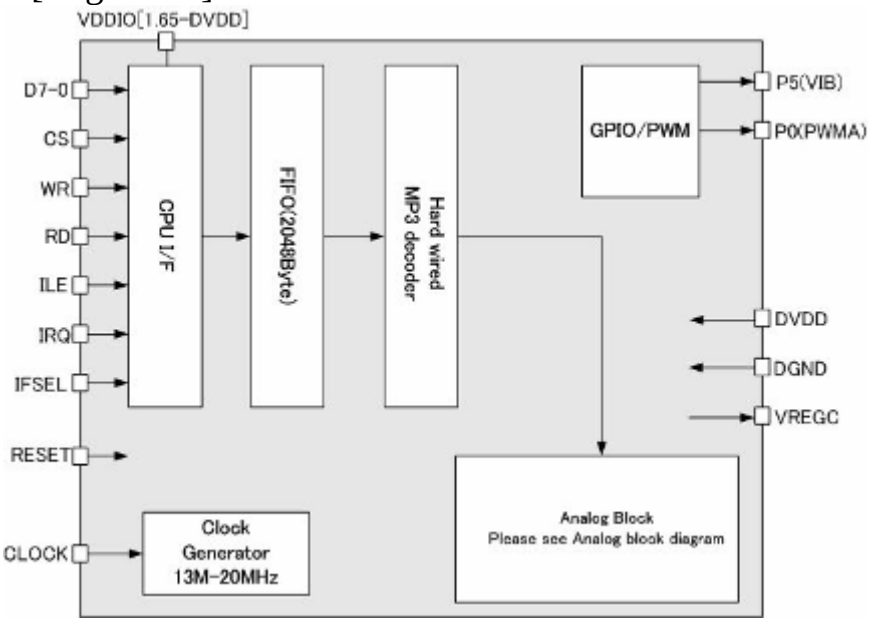
10) Package Option:
   32-pin QFN (P-VQFN0506-32)
   35-pin W-CSP (P-VFLGA35-3.56X4.56-0.50-W)

11) Operating Temperature: -20 ~ +85ºC

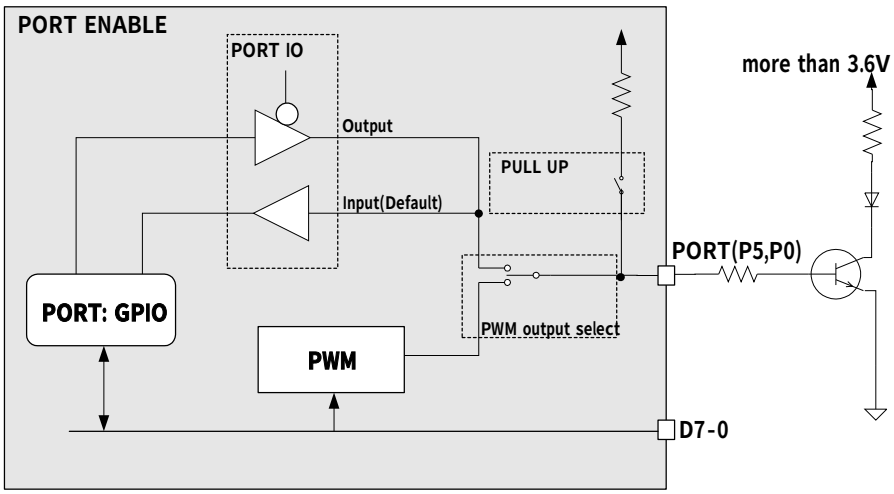
12) Provide Design Support Tools
   -Reference Board: The evaluation board including the ML2011. It can be connected user target application evaluation environment via CPU interface
   -Control software: Provide reference control software.
   Please ask OKI sales person or sales representative for more informations.

Block Diagram

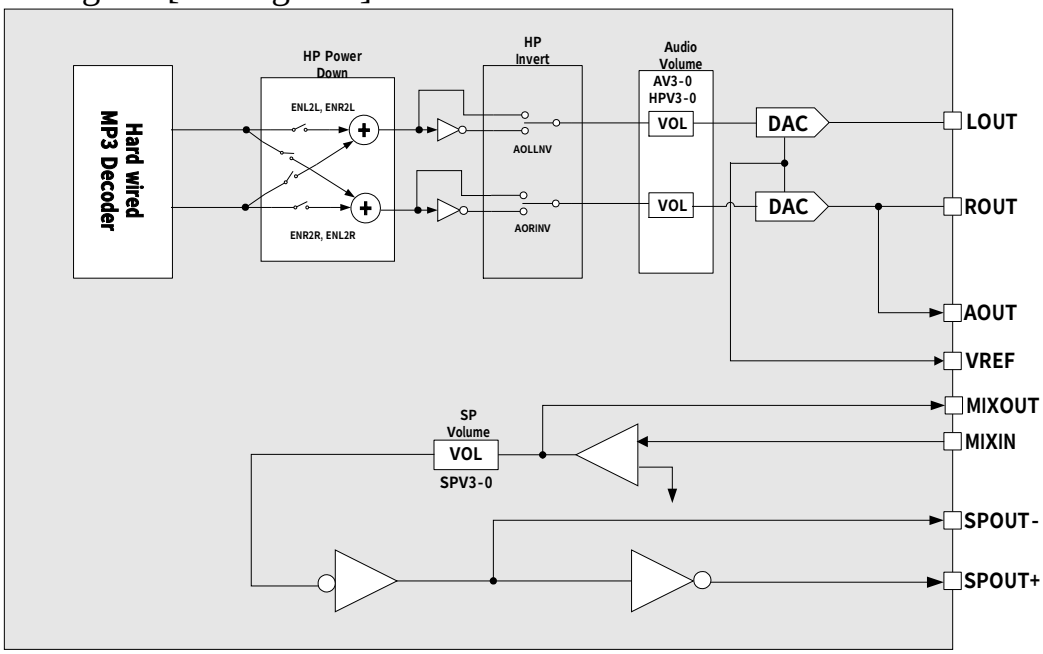
Block Diagram [Logic Part]



Block Diagram [GPIO]

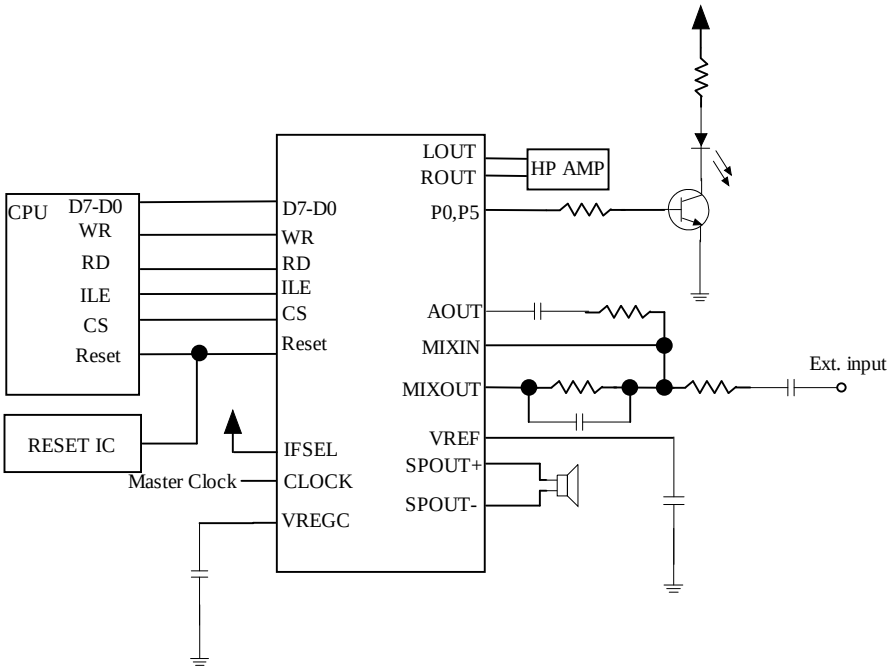


Block Diagram [Analog Part]



Typical Application Example

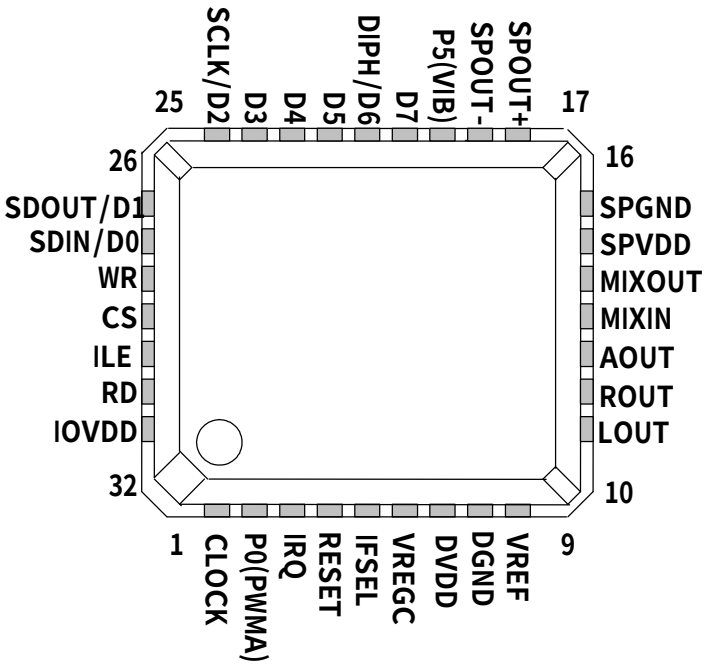
The following schematic is shown below as recommendation.



Pin Layout

32PIN QFN

TOP VIEW

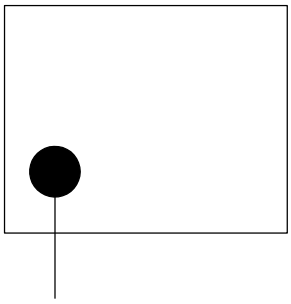


35PIN WCSP (0.5mm pitch)

Bottom View

D2	D4	D5	P5(VIB)	SPOUT-	SPOUT+	**6**
D1	D3	D6	SPGND	SPGND	(NC)	**5**
WR	D0	D7	SPGND	MIXOUT	SPVDD	**4**
CS	ILE	IFSEL	SPGND	AOUT	MIXIN	**3**
IOVDD	RD	IRQ	ROUT	DGND	LOUT	**2**
CLOCK	P0(PWMA)	RESET	VREGC	DVDD	VREF	**1**
F	**E**	**D**	**C**	**B**	**A**	

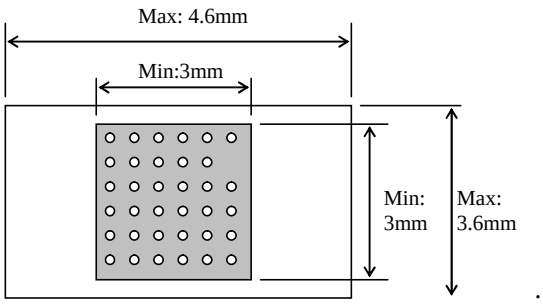
Top View



Pin A1

NOTE

Please keep PCB area for Maximum size, when product will be replaced



Pin Description

The pin description is separated into parallel, and serial interface mode and some pins can used in both mode.
If you use the parallel interface, please refer to “Description of Common mode”, “Description of Analog Pin” and “Parallel Access Mode”.
If you use the serial interface, please refer to “Description of Common mode”, “Description of Analog Pin”and “Serial Access Mode”.

Description of Common Mode

WCSP	QFN	PIN NAME	VDD	Description
D1	4	RESET	IOVDD	Hardware reset pin. When the pin is low level, LSI is in reset status. After power supply, LSI must be reset by this pin.
D2	3	IRQ	IOVDD	Interrupt request pin. This pin becomes “H”(in case ISS is 0) when interrupts occurred. CPU will access the Interrupt Request Register and check the interrupt source after interrupt occurs. When all interrupt sources are cleared, this pin becomes “L” (in case ISS is 0). When set ISS bit of the Interrupt Enable Register to “H”, the polarity of the interrupt is inverted.
D3	5	IFSEL	DVDD	IFSEL changes the CPU interface mode. CPU interface assumes bus mode, when “H”. CPU interface assumes serial mode, when “L”. * The pin has a built-in pull-up resistor. When the pin is “L” and LSI is in power down mode, pull-up resistor is not available for saving current consumption.
F1	1	CLOCK	DVDD	Master clock input. Accepts frequencies from 2.7MHz to 34MHz
C6,E1	19,2	P5, P0	IOVDD	Two functions are associated. One expands external ports for the CPU. Another is PWM output for control LED and Vibrator.
B1	7	DVDD	-	The DIGITAL power supply pin. Insert a 0.1 µF or larger by-pass capacitor between the DGND and this pin.
B2	8	DGND	-	The DIGITAL ground pin.
F2	32	IOVDD	-	The IO power supply pin. Insert a 0.1 µF or larger by-pass capacitor between the DGND and this pin.
C1	6	VREGC	-	VREGC pin should be connected to a capacitor for internal power supply. Insert a 1 µ F capacitor between the DGND and this pin.

Description of Analog Pins

WCSP	QFN	PIN NAME	VDD	Description
A6	17	SPOUT+	SPVDD	This pin is positive output for speaker output.
B6	18	SPOUT-	SPVDD	This pin is negative output for speaker output
A1	9	VREF	DVDD	This pin outputs reference voltage of internal analog circuit. It is necessary to connect 1μF capacitor between this pin and DGND pin.
A2	10	LOUT	DVDD	Left channel output pin for stereo.
C2	11	ROUT	DVDD	Right channel output pin for stereo.
B3	12	AOUT	DVDD	This pin is for audio output.
A3	13	MIXIN	DVDD	Speaker amplifier input pin.
B4	14	MIXOUT	DVDD	Output pin for Speaker input buffer
A4	15	SPVDD	-	The Speaker driver power supply pin. Insert a 0.1 μF or larger by-pass capacitor between the SPGND and this pin.
B5,C3 C4,C5	16	SPGND	-	The Speaker driver ground pin.

Parallel Access Mode

WCSP	QFN	PIN NAME	VDD	Description
D4,D5 D6,E6 E5,F6 F5,E4	20,21, 22,23, 24,25, 26,27	D7-D0	IOVDD	When ILE pin is “H”, D7-0 allow input to INDEX for register addresses. When ILE pin is “L”, D7-0 allow input and output to INDEX for register addresses.
E3	30	ILE	IOVDD	Sets the mode of D7-0 pins to index data when ILE is “H”. Data input/output from D7-0 is enabled, when ILE is “L”.
F4	28	WR	IOVDD	Write pulse input pin. This pin must be set to “L”, when index and data is input to D7-0.
E2	31	RD	IOVDD	Read pulse input pin. This pin must be set to “L”, when data is output from D7-0.
F3	29	CS	IOVDD	Write and read pulses are accepted when this pin is “L”. “H” prohibits the inputs.

Serial Access Mode

WCSP	QFN	PIN NAME	VDD	I/O	Description
E4	27	SDIN	IOVDD	I	Serial data input pin.
F5	26	SDOUT	IOVDD	O	Serial data output pin.
F6	25	SCLK	IOVDD	I	Input pin of the data synchronization clock for the SDIN and SDOUT pins.
F3	29	CS	IOVDD	I	Chip select input. When “L” the SCLK data clock is accepted. The SCLK data clock is prohibited when CS=“H”.
D5	21	DIPH	IOVDD	I	DIPH pin defines timing which the SDIN data is latched by SCLK. Input timing of serial interface depends on the SCLK level when CS pin is altering to “L” and the DIPH pin level. Please look at the timing chart of serial interface for detailed information.
E2,F4 E3	31,28, 30	(RD),(WR), (ILE)	IOVDD	I	Unused pins. Please connect to GND level
D4	20	(D7)	IOVDD	I	Unused pins. It must be connected to GND level.
D6,E5 E6	22,23 24	(D3),(D4), (D5)	IOVDD	O	Unused pins. Please keep is open.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply votage 1	DV_{DD}	-	-0.3 - +5.0	V
Supply votage 2	SPV_{DD}	-	-0.3 - +6.5	V
Input voltage	V_{IN}	-	-0.3 - IOV_{DD}+0.3	V
Output Current*1	Io	-	-8 - +8	mA
Power dissipation*2	Pd	-	805	mW
Storage temperature	T_{STG}	Ta=25°C	-55 - +125	°C

NOTE:

*1 Apply to output/input or output pins other than SPOUT+/SPOUT-,LOUT,ROUT.AOUT,MIXOUT
Note): Please don't short circuit the output pin, or short circuit the output pin with the GND.(Output pins include the input/output pins operating under output mode.)

*2 Please refer to Power Derating Curves for detailed information.

Recommended Operating Condition

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	DV_{DD}	DGND=SPGND=0V	2.7 – 3.6	V
Supply Voltage	SPV_{DD}	DGND=AGND=0V	DVDD – 4.5	V
Supply Voltage	IOV_{DD}	DGND=AGND=0V Bus Interface	1.65-DVDD	V
Supply Voltage	IOV_{DD}	DGND=AGND=0V Serial Interface	DVDD	V
Operating Temperature	T_{OP1}	Please refer to Power Derating Curves.	-20 -+85	°C
Operating Temperature	T_{OP2}	Speaker amplifier is not used.	-20 -+85	°C
Operating Junction Temperature	T_j	-	Max 125	°C
Master clock frequency	f_{CLK}	-	2.7- 34	MHz

Electrical Characteristics

DC Charactaristics

IOVDD=1.65-DVDD, DVDD =2.7V-3.6V, SPVDD=DVDD-4.5V
DGND=SPGND=0V, Ta=-20-+85°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Input Voltage Except IFSEL, CLOCK	VIH	DGND=AGND=0V	IOVDD x 0.8	-	IOVDD + 0.3	V
"L" Input Voltage Except IFSEL, CLOCK	VIL	-	-0.3	-	IOVDD x 0.2	V
"H" Input Voltage Apply to IFSEL, CLOCK	VIH2	DGND=AGND=0V	DVDD x 0.8	-	DVDD + 0.3	V
"L" Input Voltage Apply to IFSEL, CLOCK	VIL2	-	-0.3	-	DVDD x 0.2	V
"H" Output Voltage except P5,P0	VOH	IOH=-135μA	VDDx0.8	-	-	V
"L" Output Voltage except P5,P0	VOL	IOL=135μA	-	-	IOVDDx0.2	V
"H" Output Voltage2 Apply to P5,P0	VOH2	IOH=-5mA IOVDD>= 2.7V	IOVDDx0.8	-	-	V
		IOH=-135μA IOVDD< 2.7V	IOVDDx0.8			V
"L" Output Voltage2 Apply to P5,P0	VOL2	IOL=5mA IOVDD>= 2.7V	-	-	IOVDDx0.2	V
		IOL=135μA IOVDD< 2.7V	-	-	IOVDDx0.2	V
"H" Input Current	IIH	VIH=VDD	-	-	10	μA
"L" Input Current	IIL	VIL=0V	-10	-	-	μA
Master clock voltage in front of an AC coupling capacity to the CLOCK pin	VCLK	AC coupling capacity depends on frequency.	400	-	-	mVp-p
IFSEL pin Pull-Up resistor value	RT1	- *1	20	100	200	kΩ
P5,P0 pin Pull-Up resistor value	RT2	-	20	100	500	kΩ

NOTE
*1 When serial I/F mode is selected or LSI is in power down state, pull-up resister is removed for saving power.

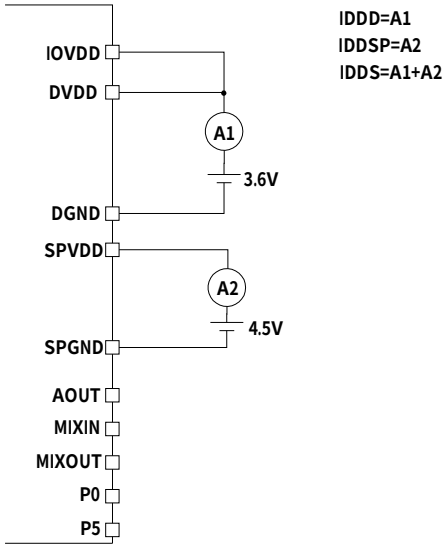
Current Consumption

(IOVDD=1.8V, LVDD=2.5V, HVDD=4.2V, Ta=25°C, no-load, no-signal, PLL off)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
DVDD Operating Current	IDDD	Ports: no load AOUT pins : enable / no-load *1		-	27	45	mA
SPVDD Operating Current 1	IDDSP1	DVDD=3.0V,SPVDD=3.6V No-load		-	5	-	mA
SPVDD Operating Current 2	IDDSP2	DVDD=3.0V,SPVDD=3.6V RSP=8Ω Playing Data:sin1k.mp3		-	210	-	mA
Standby Current	IDDS	DVDD≤3.6V SPVDD≤4.5V	Ta=-20-+40°C	-	2	18	μA
			Ta=+40-+50°C	-	-	35	μA
			Ta=+50-+75°C	-	-	190	μA
			Ta=+75-+85°C	-	-	380	μA

NOTE

*1 The following figure shows the measurement circuit.



AC Charactaristics

Reset Timing

IOVDD=1.65-DVDD, DVDD=2.7V-3.6V, SPVDD=DVDD-4.5V
DGND=SPGND=0V, Ta=-20-+85°C

Parameter	Symbol	Min.	Max.	Unit
RESET pulse width	tRST	1	-	μs
CSB valid to RESET High	tINIT	1	-	μs

Bus Interface at Write Cycle

IOVDD=1.65-DVDD, DVDD=2.7V-3.6V, SPVDD=DVDD-4.5V
DGND=SPGND=0V, Ta=-20-+85°C, Capacitor Load=30pF

Parameter	Symbol	Min.	Max.	Unit
CSN setup time	tSU_CSN	50	-	ns
CSN hold time	tH_CSN	0	-	ns
ILE setup time	tSU_ILE	0	-	ns
ILE hold time	tH_ILE	0	-	ns
Data setup time	tSU_D	50	-	ns
Data hold time	tH_D	0	-	ns
WRN Low pulse width	tW_WRN	25	-	ns
Cycle time of WRN	tCYC_WRN	100	-	ns

Bus Interface at Read Cycle

IOVDD=1.65-DVDD, DVDD=2.7V-3.6V, SPVDD=DVDD-4.5V
DGND=SPGND=0V, Ta=-20-+85°C, Capacitor load=30pF

Parameter	Symbol	Min.	Max.	Unit
CSN setup time	tSU_CSN	50	-	ns
CSN hold time	tH_CSN	0	-	ns
RDN Low pulse width	tW_RDN	85	-	Ns
Data delay	tD_D	-	70	ns
Data Hi-Z delay	tDZ_D	-	70	ns

Serial Interface

IOVDD=DVDD=2.7V-3.6V, SPVDD=DVDD-4.5V
DGND=SPGND=0V, Ta=-20-+85°C

Parameter	Symbol	Min.	Max.	Unit
SCLK Low to Chip Select enable	tSLCL	100	-	ns
Chip Select enable to SCLK Low	tCLSL	50	-	ns
Chip Select enable to SCLK High	tCLSH	100	-	ns
SCLK High to Chip Select enable	tSHCL	50	-	ns
SCLK High Pulse Width	tSH	50	-	ns
SCLK Low Pulse Width	tSL	50	-	ns
Input Data Hold time	tIDH	30	-	ns
Input Data Setup time	tIDS	30	-	ns
SCLK last edge to Chip Select disable	tCHS1	0	-	s
SCLK last edge to Chip Select disable	tCHS2	100	-	ns
Chip Select High Pulse Width	tCH	50	-	ns
Output Data Valid	tODV	-	40	ns
Chip Select High to Data Transition	tCHDTS	-	40	ns

Analog Charactaristics

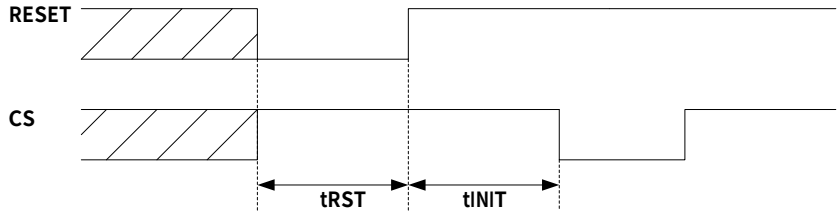
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply voltage range	VDD	-	2.7	3.0	3.6	V
Power Supply voltage range	SPVDD	-	2.7	3.6	4.5	V
Operating temperature range	Ta	-	-20	25	85	℃
L/R/AOUT Output	VOUT	DAC Input：Sin 1kHz, ROUT=10 kΩ	1.29	1.43	1.58	Vp-p
MIXOUT	VMIX	DAC Input：Sin 1kHz, RMIX=10 kΩ	1.29	1.43	1.58	Vp-p
SP Output	VSP	DAC Input：Sin 1kHz, RSP=8 kΩ	5.8	-	-	Vp-p
Operating Frequency Limit	fOUT	-	-	-	20	kHz
L/R/AOUT allowable load	ROUT	-	10	-	-	kΩ
MIXOUT allowable load	RMIX	-	10	-	-	kΩ
SPOUT allowable load	RSP	-	8	-	-	Ω
VREGC external capacitor	CVREGC	-	0.6	1	1.5	μF
VREF external capacitor	CVREF	-	0.6	1	1.5	μF

Timing Chart

Operation of Power On

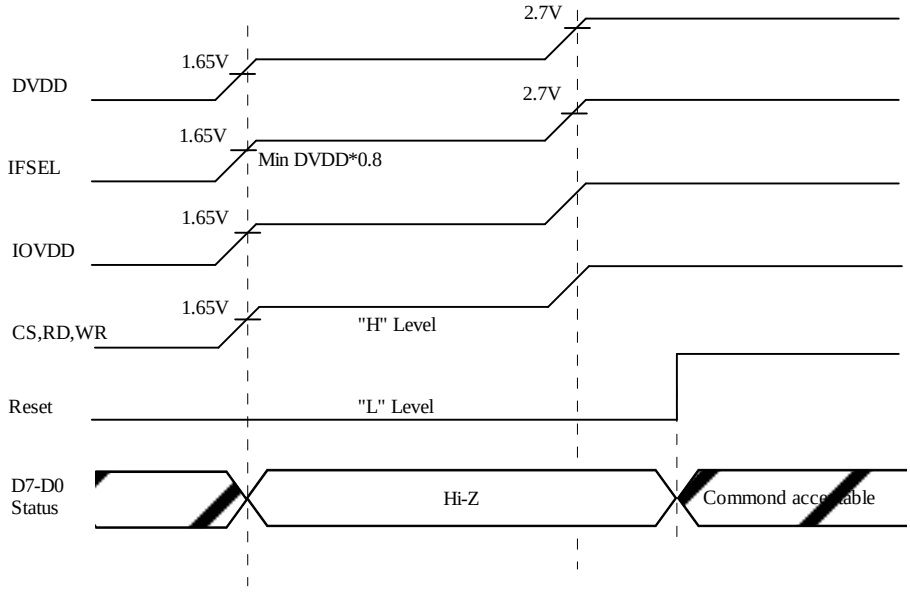
To initialize the LSI, minimum 1 micro second "Low level" must be applied to the Reset pin. After releasing the reset, the internal circuits initialize. After the initialization, register is set with default value and MP3 FIFO is empty.

Sequencer for raising VDD



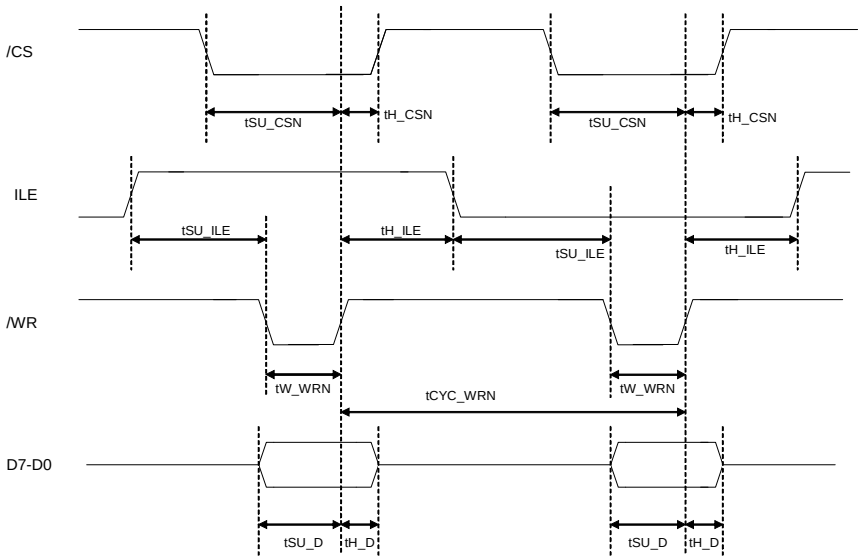
Data-Bus status at Power On

Data-Bus becomes high impedance under such conditions.
Condition: DVDD >= IOVDD=1.65V , IFSEL >= DVDD*0.8



Bus Interface Sequencer

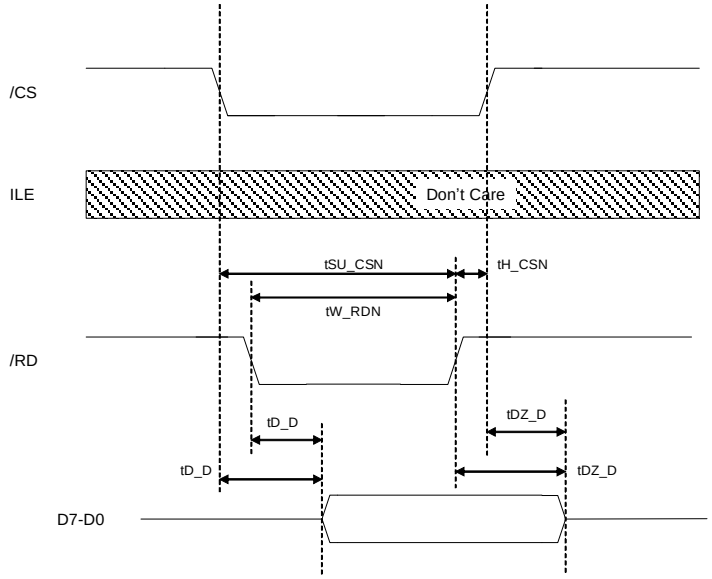
DATA Write Timing



8bit-Parallel Write Waveform

Note: tSU_D, tH_D are defined with respect to the moment /CS or /WR become high level.

Data Read Timing



8bit-Parallel Read Waveform

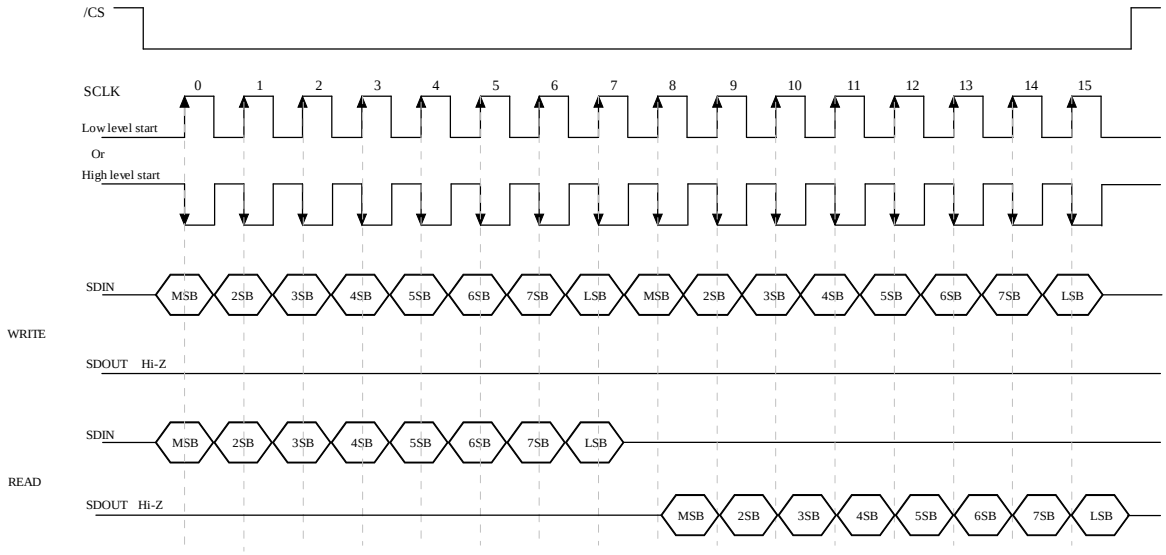
(Measurement condition) VOH=0.8*IOVDD, VOL=0.2*IOVDD

Serial Interface Sequencer

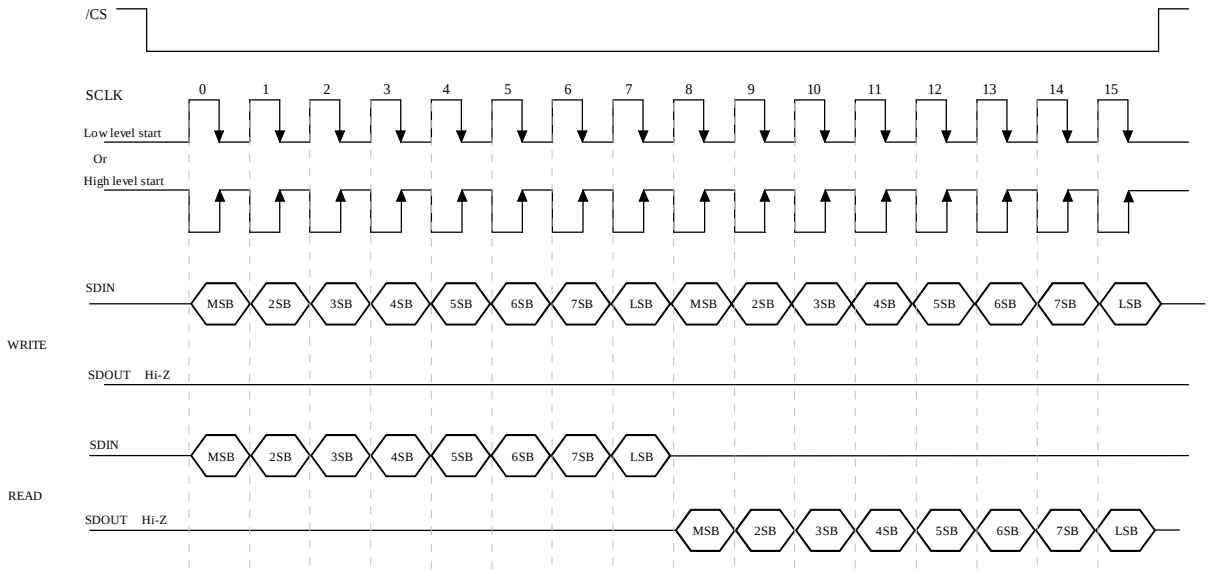
Phase controll with SDIN and SDOUT

Serial interface mode has two data transmission timing by DIPH level. First edge transmission is transmitted data in synchronization with first edge of SCLK when DIPH is forced "High level". Similarly, last edge transmission is transmitted data in synchronization with last edge when DIPH is forced "Low level". Data writing edge is decided by the SLCK level when the /CS is enable.

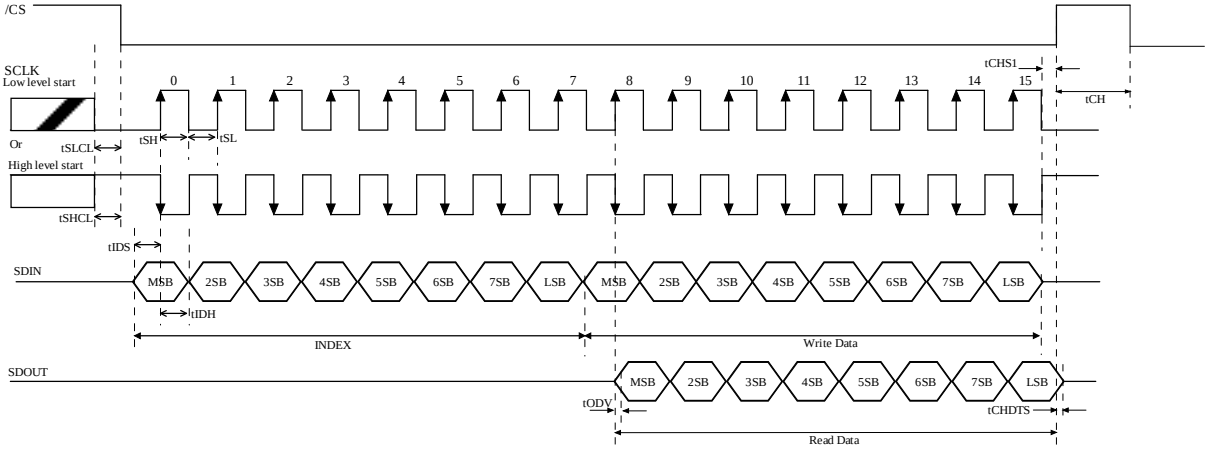
First edge data transmission (DIPH = "High")



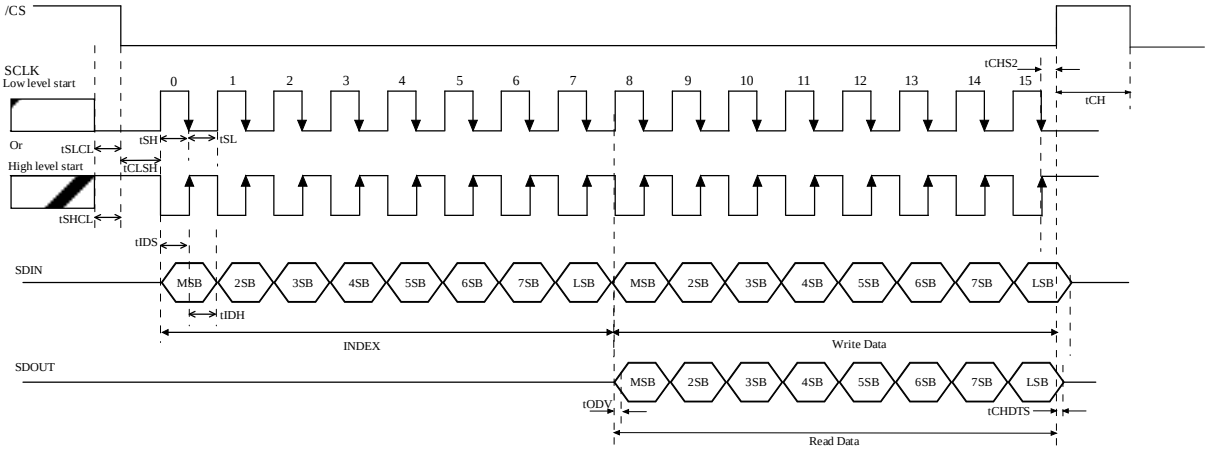
Last edge transmission (DIPH = "Low")



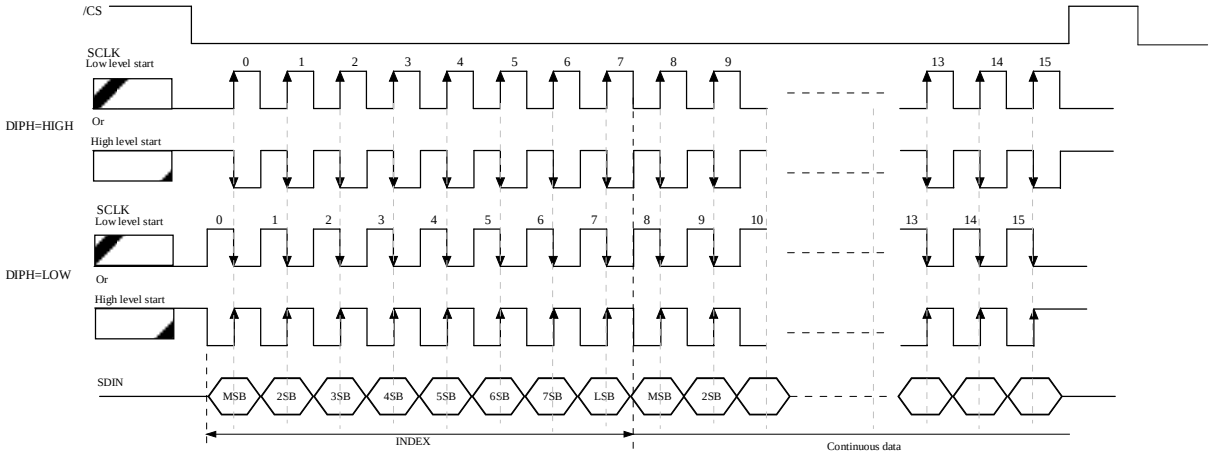
Data Write & Read Timing in case of DIPH = "High"



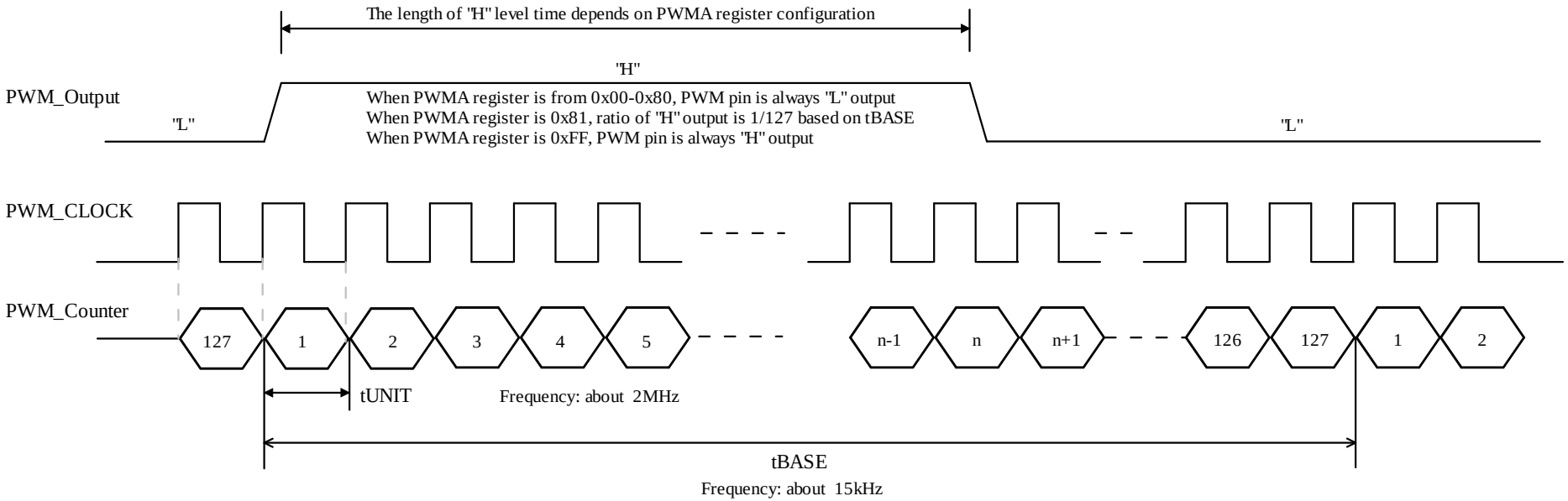
Data Write & Read Timing in case of DIPH = "Low"



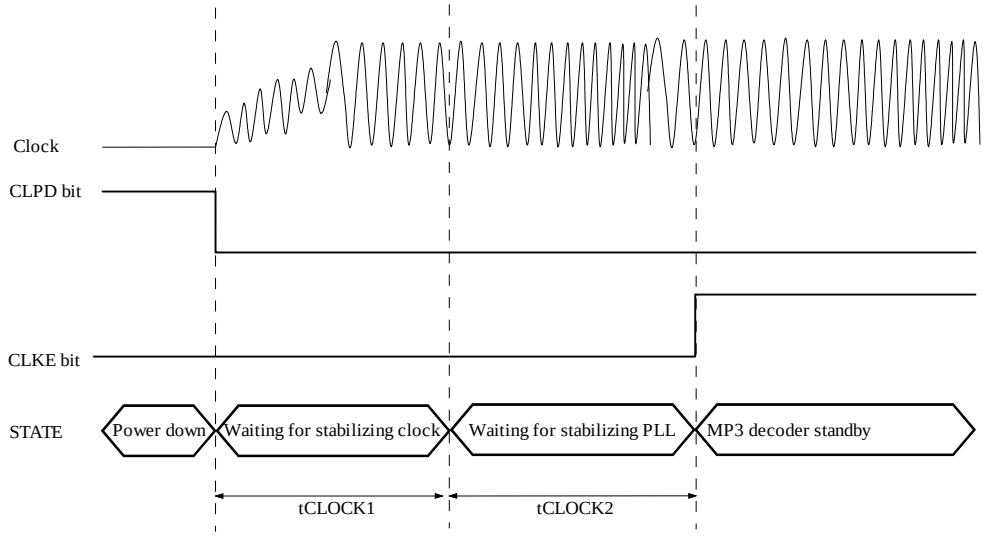
Continuous data transfer to FIFO



Timing chart of PWM output

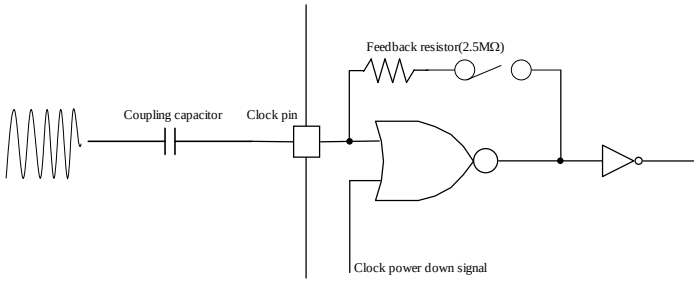


Power up Timing (Reset Power Down)

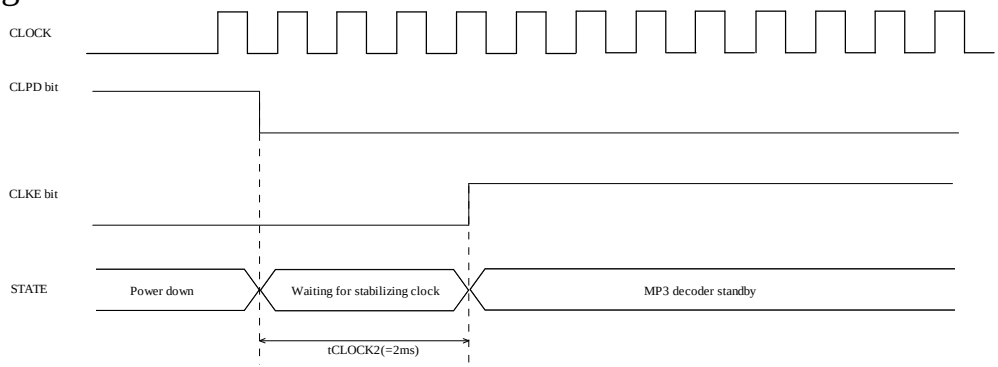


- Before the PLL operation, ML2011 needs "tCLOCK1" to stabilize signal.
- When ML2011 connected to small range clock signal, the AC coupling capacitor determines the value of "tCLOCK1".

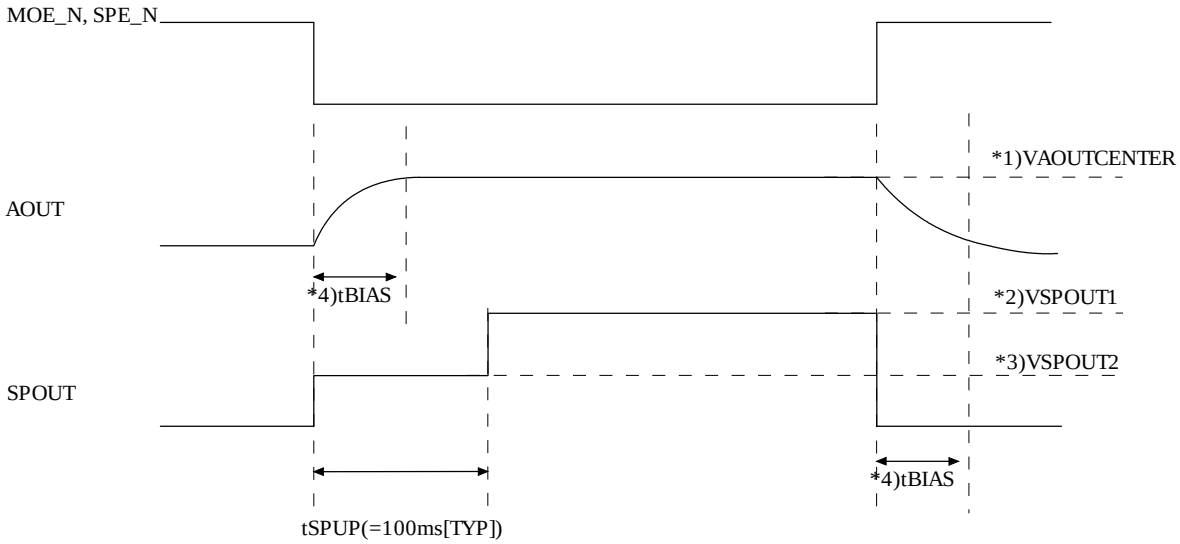
Capacitor	tCLOCK1 (MAX)
100pF	0.5ms
1000pF	5ms
0.01μF	50ms
0.1μF	500ms



Digital signal clock source



Timing chart of analog power down

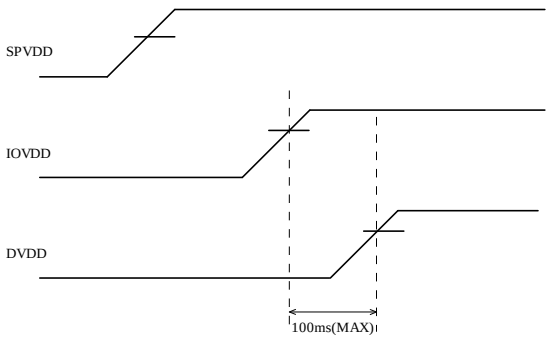


*1) VAOUTCENTER(TYP)=VREF [V]
*2) VSPOUT1(TYP)=VREFx1.47 [V]
*3) VSPOUT2(TYP)=VREFx0.81 [V]
*4) tBIAS(TYP)= 2π x Cinput x 35 x 10^3 [s]

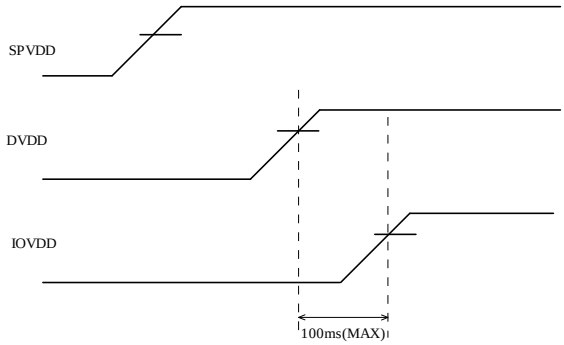
Power supply

Timing Chart of Supplying Raising Power Supply

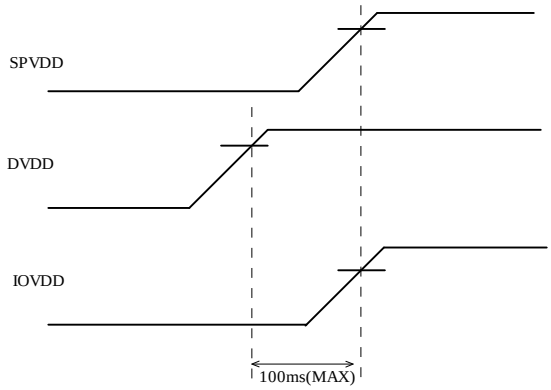
Case 1



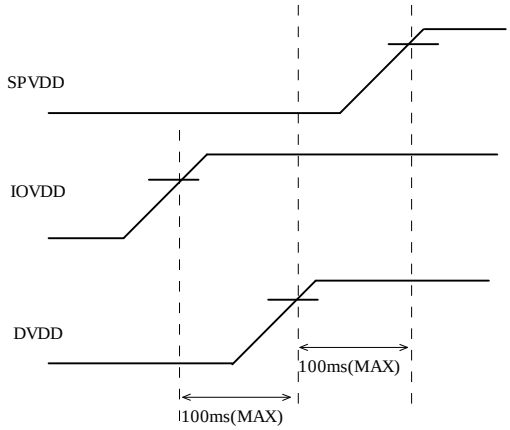
Case 2



Case 3



Case 4



Functional Description of THE REGISTERS

Register Map 1

FIFO Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
	$01h	d07 0	d06 0	d05 0	d04 0	d03 0	d02 0	d01 0	d00 0	MP3 FIFO
$02h		- -	- -	- -	- -	- -	FULL 0	THR 1	EMP 1	MP3 FIFO Status
	$05h	- -	- -	- -	- -	- -	- -	- -	CLR 0	MP3 FIFO Clear
MP3 Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$06h	$07h	- -	- -	- -	- -	- -	- -	OUT 0	STA 0	MP3 Control
$08h	$09h	- -	- -	- -	- -	- -	- -	CS1 0	CS0 0	MP3 dual channel select
$0Ah	$0Bh	TH7 0	TH6 0	TH5 0	TH4 0	TH3 0	TH2 0	TH1 0	TH0 0	MP3 FIFO threshold0
$0Ch	$0Dh	- -	- -	- -	- -	- -	TH10 0	TH9 0	TH8 0	MP3 FIFO threshold1
$0Eh		- -	- -	- -	- -	RQ3 0	RQ2 0	RQ1 0	RQ0 0	MP3 FIFO requested data 0
$10h		RQ11 1	RQ10 0	RQ9 0	RQ8 0	RQ7 0	RQ6 0	RQ5 0	RQ4 0	MP3 FIFO requested data 1
$12h	$13h		- -	- -	- -	- -	ISR 0	ILR 0	IBR 0	MP3 ERROR
$14h	$15h		-	-	-	-	NFRM	IFEMP	STP	MP3 WARNING
			-	-	-	-	0	0	0	
$16h	$17h	- -	- -	- -	- -	- -	- -	OBUF 0	BUSY 0	MP3 STATUS
$18h		- -	- -	- -	- -	PAD 0	CRC 0	PLY1 0	PLY0 1	MP3 format register0
$1Ah		FRQ3 0	FRQ2 0	FRQ1 0	FRQ0 0	BT3 0	BT2 0	BT1 0	BT0 0	MP3 format register1
$1Ch		EP1 0	EP0 0	ORID 0	CPRT 0	EXM1 0	EXM0 0	MOD1 0	MOD0 0	MP3 format register2
$1Eh	$1Fh	- -	- -	- -	- -	- -	- -	- -	DRQSEL 0	MP3 Data Request Select

Note: "-" represents reserved values. 0 will be returned when reading the values, and the writing to these value will be neglected. Please ignore these values in software.

Register Map 2

LSI Control Register											
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$20h	$21h	- -	- -	- -	CLPD 0	CLKE 0	- -	- -	- -	Power Down
$22h	$23h	PLL2 0	PLL1 0	PLL0 0	CK4 0	CK3 0	CK2 0	CK1 0	CK0 0	Clock
$24h	$25h	- -	- -	PL2DIV5 0	PL2DIV4 0	PL2DIV3 0	PL2DIV2 0	PL2DIV1 0	PL2DIV0 0	PLL2 Clock Division
$26h	$27h	- -	- -	64DIV5 0	64DIV4 0	64DIV3 0	64DIV2 0	64DIV1 0	64DIV0 0	64KAudioClock Division
$28h	$29h	- -	64MUL6 0	64MUL5 0	64MUL4 0	64MUL3 0	64MUL2 0	64MUL1 0	64MUL0 0	64KAudioClock Multiple
$2Ah	$2Bh	- -	- -	88DIV5 0	88DIV4 0	88DIV3 0	88DIV2 0	88DIV1 0	88DIV0 0	88KAudioClock Division
$2Ch	$2Dh	- -	88MUL6 0	88MUL5 0	88MUL4 0	88MUL3 0	88MUL2 0	88MUL1 0	88MUL0 0	88KAudioClock Multiple
$2Eh	$2Fh	- -	- -	96DIV5 0	96DIV4 0	96DIV3 0	96DIV2 0	96DIV1 0	96DIV0 0	96KAudioClock Division
$30h	$31h	- -	96MUL 6 0	96MUL5 0	96MUL4 0	96MUL3 0	96MUL2 0	96MUL1 0	96MUL0 0	96KAudioClock Multiple
$32h	$33h	FEED 0	- -	- -	- -	- -	- -	- -	- -	Ext Clock Control
$34h	$35h	- -	- -	- -	- -	- -	- -	- -	SRST 0	Soft Reset
Interrupt Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$38h	$39h	ISS 0	PLKE 0	ENDE 0	FRME 0	WARNE 0	ERRE 0	DRQE 0	MONE 0	Interrupt Enable
$3Ah	$3Bh	- -	PLK 0	ENDST 0	FRMST 0	WARNST 0	ERRST 0	FIFODRQST 1	MONST 0	Interrupt request

Note: "-" represents reserved values. 0 will be returned when reading the values, and the writing to these value will be neglected. Please ignore these values in software.

Register Map 3

Port Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$42h	$43h	-	-	PIO5 0	-	-	-	-	PIO0 0	Port IO
$44h	$45h	- -	- -	P5 ?	- -	- -	- -	- -	P0 ?	Port
$48h	$49h	WAE 0	WA6 0	WA5 0	WA4 0	WA3 0	WA2 0	WA1 0	WA0 0	PWMA
$52h	$53h	WVE 0	WV6 0	WV5 0	WV4 0	WV3 0	WV2 0	WV1 0	WV0 0	VIB
$54h	$55h	- -	- -	PUP5 1	- -	- -	- -	- -	PUP0 1	Pull up(Port)
$56h	$57h	-	-	P5 0	-	-	-	-	P0 0	PWM Output select
$58h	$59h	-	-	P5E	-	-	-	-	P0E	Port Enable
				1					1	
Analog Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$62h	$63h	HPV3 0	HPV2 1	HPV1 0	HPV0 0	AV3 0	AV2 1	AV1 0	AV0 0	Audio Volume
$64h	$65h	- -	- -	- -	- -	SPV3 0	SPV2 0	SPV1 0	SPV0 0	SP Volume
$66h	$67h	BIASL 0	PDL 1	ENR2L 1	ENL2L 1	BIASR 0	PDR 1	ENL2R 1	ENR2R 1	HP Power down
$68h	$69h	-	-	-	-	-	-	LINV 0	RINV 0	HPOUT Invert
$6Ah	$6Bh	-	-	-	-	-	-	MOE_N 1	SPE_N 1	Analog PowerDown
Product Identification Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$F0h		ID7 1	ID6 0	ID5 0	ID4 0	ID3 0	ID2 0	ID1 0	ID0 0	Product ID

Note: "-" represents reserved values. 0 will be returned when reading the values, and the writing to these value will be neglected. Please ignore these values in software.

"?" represents that the initial value of the Port Register is related to the system.

The status of the registers in according to Software reset, Hardware reset, during Powerdown, after Powerdown.

The following table desribes the difference of registers under different conditions.

Registers/ Functions	Register Name	RESET Pin	Soft Reset	During CLPD=1	After clearing CLPD bit
Registers	MP3 FIFO	Read inhibit	Read inhibit	Read inhibit	Read inhibit
	MP3 FIFO Status	Reset	Reset	0	Reset
	MP3 FIFO Clear	Read inhibit	Read inhibit	Read inhibit	Read inhibit
	MP3 Control	Reset	0	0	0
	MP3 dual channel select	Reset	No Change	No Change	No Change
	MP3 FIFO threshold0	Reset	Reset	0	Reset
	MP3 FIFO threshold1	Reset	Reset	0	Reset
	MP3 FIFO reqested data 0	Reset	Reset	0	Reset
	MP3 FIFO reqested data 1	Reset	Reset	0	Reset
	MP3 ERROR	Reset	Reset	0	Reset
	MP3 WARNING	Reset	Reset	0	Reset
	MP3 STATUS	Reset	Reset	0	Reset
	MP3 format register0	Reset	Reset	0	Reset
	MP3 format register1	Reset	Reset	0	Reset
	MP3 format register2	Reset	Reset	0	Reset
	MP3 Data Request Select	Reset	Reset	0	Reset
	Power Down	Reset	No Change	Powerdown (CLPD=1, CLKE=0)	PowerUp (CLPD=0, CLKE=0)
	Clock	Reset	No Change	No Change	No Change
	PLL2 Clock Division	Reset	No Change	No Change	No Change
	64K Audio Clock Division	Reset	No Change	No Change	No Change
	64K Audio Clock Multiple	Reset	No Change	No Change	No Change
	88K Audio Clock Division	Reset	No Change	No Change	No Change
	88K Audio Clock Multiple	Reset	No Change	No Change	No Change
	96K Audio Clock Division	Reset	No Change	No Change	No Change
	96K Audio Clock Multiple	Reset	No Change	No Change	No Change
	Ext Clock Control	Reset	No Change	No Change	No Change
	Soft Reset	Reset	0 (Clear SRST)	0	Reset
	Interrupt Enable	Reset	No Change	0 (except ISS bit)	Reset (except ISS bit)
	Interrupt request	Reset	Reset	0	Reset
	Port IO	Reset	Reset	No Change	No Change
	Port	Reset	Reset	Accoding to Register setting	Accoding to Register setting
	PWMA	Reset	Reset	No Change	No Change
	VIB	Reset	Reset	No Change	No Change
	Pull up(Port)	Reset	No Change	No Change	No Change
	PWM Output select	Reset	Reset	No Change	No Change
	Port Enable	Reset	Reset	No Change	No Change
	Audio Volume	Reset	Reset	No Change	No Change
	SP Volume	Reset	Reset	No Change	No Change
	HP Power down	Reset	Reset	No Change	No Change
	HPOUT Invert	Reset	Reset	No Change	No Change
	Analog Power Down	Reset	Reset	No Change	No Change
	Product ID	No Change	No Change	No Change	No Change
Functions	MP3 Decoder	Reset	Reset	Power Down	Reset
	PWM	Reset	Reset	Power Down	Reset

Detailed Description of the Registers

MP3 FIFO Register (Read : inhibit / Write : $01h)

FIFO Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
	$01h	d07 0	d06 0	d05 0	d04 0	d03 0	d02 0	d01 0	d00 0	MP3 FIFO

The register is used to input MP3 data.

When playing MP3, the LSI reads and erases data in MP3 FIFO at the same time.
As defined in the MP3 Data Request Select Register, the LSI outputs a interrupt signal when the data in the MP3 FIFO lower than the pre-defined threshold, or when the MP3 decoder requests data. Write the next MP3 data when the FIFODRQST bit in Interrupt request register has been resetted.

MP3 FIFO Status Register(Read $02h : / Write : inhibit)

FIFO Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$02h		- -	- -	- -	- -	- -	FULL 0	THR 1	EMP 1	MP3 FIFO status

This register shows the status of the MP3 FIFO.

EMP bit: Indicates the MP FIFO is empty or not.

EMP	Describtion
0	FIFO is not empty
1	FIFO is empty

THR bit: Indicates if the data amount is higher than the threshold defined in MP3 FIFO threshold0,1 register.

THR	Description
0	Data amount in FIFO is high than threshold
1	Data amount in FIFO is less than threhold

FULL bit: Indicates that if the MP3 FIFO is full or not. In full status, any writing attempt to FIFO will be neglected.

FULL	Description
0	FIFO is full
1	FIFO is not full

MP3 FIFO Clear Register (Read: - / Write : $05h)

FIFO Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
-	$05h	- -	- -	- -	- -	- -	- -	- -	CLR 0	MP3 FIFO Clear

This register is used to clear MP3 FIFO and to initialize MP3 decoder.

When CLR bit is set to “1”, the MP3 FIFO will be cleared and at the same time, the MP3 decoder will be initialized. Please execute this operation when start to play MP3 music.

MP3 Control Register(Read $06h : / Write : $07h)

MP3 Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$06h	$07h	- -	- -	- -	- -	- -	- -	OUT 0	STA 0	MP3 Control

This register is used to control the operation of MP3 decoder.

STA bit：Control the start and Stop of MP3 decoder. Please set the STA bit to 1 after writing data in MP3 FIFO, and the MP3 decoder will start to decode the data in FIFO.

STA	Description
0	MP3 stop decoding
1	MP3 start to decode

OUT bit：Control the output of MP3 decoder. When set to STA, and decoder start decoding, please set to OUT after the following conditions are prepared.

Decoder detects the synchronized character in the mp3 music.
MP3 FIFO is not empty(The EMP bit of MP3 FIFO status register is “0”)
The output buffer status of MP3 decoder is full(The OBUF bit of MP3STAT register is “1”)
PLL2 is locked(The PLK bit of Interrupt request register is “1”)

After setting OUT, sound will be outputted if there is any effective data exists in the PCM output buffer in the MP3 decoder. And it will be in silent mode if no effective data exists.
To pause mp3 playing, set OUT to 0.

OUT	Description
0	Stop outputting the PCM data in MP3 decoder
1	Start outputting the PCM data in MP3 decoder

MP3 Dual Channel Select Register (Read $08h: / Write : $09h)

MP3 Control Register										
INDEX		b07	b06	b05	b04	B03	b02	b01	b00	NOTE
R	W	(Initial)								
$08h	$09h	-	-	-	-	-	-	CS1	CS0	MP3 dual channel select
		-	-	-	-	-	-	0	0	

This register controls the MP3 output channel.

CS0, CS1 bit: Choose output channel when play MP3 data in dual mode. This register will be neglected when play non dual mode MP3.

CS1	CS0	Description
0	0	Two channels output at the same time
0	1	L,R channel output the main sound of L channel
1	0	L,R channel output the affiliated sound of R channel
1	1	Prohibited to set

MP3 FIFO Threshold0 Register(Read : $0Ah / Write : $0Bh)
MP3 FIFO Threshold1 Register(Read :$0Ch / Write : $0Dh)

MP3 Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$0Ah	$0Bh	TH7 0	TH6 0	TH5 0	TH4 0	TH3 0	TH2 0	TH1 0	TH0 0	MP3 FIFO threshold0
$0Ch	$0Dh	- -	- -	- -	- -	- --	TH10 0	TH9 0	TH8 0	MP3 FIFO threshold1

MP3 FIFO Threshold0,1 Register is the threshold register used to create the data request interrupt signal of MP3 FIFO.

Use TH0-TH10 to set the data request interrupt signal of MP3 FIFO. If the remaining data in MP3 FIFO is less than the threshold, the MP3 FIFO data request will be generated.

MP3 FIFO Requested Data0 Register(Read $0Eh : / Write : inhibit)
MP3 FIFO Requested Data1 Register(Read $10h : / Write : inhibit)

MP3 Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$0Eh		- -	- -	- -	- -	RQ3 0	RQ2 0	RQ1 0	RQ0 0	MP3FIFOrequested data0
$10h		RQ11 1	RQ10 0	RQ9 0	RQ8 0	RQ7 0	RQ6 0	RQ5 0	RQ4 0	MP3FIFOrequested data1

MP3 FIFO Requested Data0, 1 register represents the amount of data requested by MP3 FIFO.

Use RQ0-RQ11 to represent the amount of requested data in MP3 FIFO. When data request interrupt of MP3 FIFO occurs, the amount of data indicated by the register has to be written in MP3 FIFO.

MP3 Error Register(Read $12h : / Write : inhibit)

MP3 Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$12h	$13h	-	-	-	-	-	ISR	ILR	IBR	MP3 ERROR
		-	-	-	-	-	0	0	0	

This register represents the status of MP3 decoder.

ISR bit: represents whether the decoder detected the non-supported sampling rate. If ISR is set to “1”, it will output MP3 decoder error interrupt, and it represents that error has been occurred in MP3 decoder. If the decoder detected the sampling rate which is not supported, please stop using the decoder, and re-initialize the decoder. Write “1” to this bit can clear this bit.

ISR	Description
0	The non-supported sampling rate not be detected.
1	The non-supported sampling rate be detected.

ILR bit: represents whether the decoder detected the non-supported layer. If the ILR is set to “1”,it will output MP3 decoder error interrupt, and this indicates error has been occurred in MP3 decoder. If non-supported layer has been detected, please stop using the decoder, and reset the decoder. Write “1” to this bit can clear this bit.

ILR	Description
0	The non-supported layer not be detected.
1	The non-supported layer be detected.

IBR bit: represents whether the decoder detected the non-supported bit rate. If the IBR is set to “1”,it will output MP3 decoder error interrupt, and this indicates error has been occurred in MP3 decoder. If non-supported bit rate has been detected, please stop using the decoder, and reset the decoder. Write “1” to this bit can clear this bit.

IBR	Description
0	The non-supported bit rate not be detected
1	The non-supported bit rate be detected

MP3 WARNING Register(Read $14h : / Write : $15h)

MP3 Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$14h	$15h	-	-	-	-	-	NFRM	IFEMP	STP	MP3 WARNING
		-	-	-	-	-	0	0	0	

This register represents the warning message occurred during the mp3 playing.

NFRM bit: When MP3 decoder didn't detect any frame, this bit will be set to "1". If this bit is set to "1", the LSI will create mp3 warning message interrupt. If the upcoming normal mp3 data is inputted, the music can continue to play. This bit can be cleared by writing "1".

NFRM	Description
0	FRAME detected
1	FRAME not be detected

IFEMP bit: represents whether the data input FIFO of the internal MP3 decoder is empty or not。 If this bit is set to "1", the LSI will create mp3 warning message interrupt. If the upcoming normal mp3 data is inputted, the music can continue to play. This bit can be cleared by writing "1".

EMP	Description
0	Data input FIFO of internal MP3 decoder is not empty
1	Data input FIFO of internal MP3 decoder is empty

STP bit: represents whether any interrupt occurred in mp3 sound output. If this bit is set to "1", the LSI will create mp3 warning message interrupt. If the upcoming normal mp3 data is inputted, the music can continue to play. This bit can be cleared by writing "1".

STP	Description
0	Interrupt didn't occur in mp3 sound output
1	Interrupt occurred in mp3 sound output

MP3 STATUS Register(Read $16h : / Write : $17h)

MP3 Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$16h	$17h	-	-	-	-	-	-	OBUF	BUSY	MP3 STATUS
		-	-	-	-	-	-	0	0	

This register represents the status of mp3 decoder.

OBUF bit: represents whether the mp3 decoder output buffer is full. This bit can be cleared by writing “1”.

OBUF	Description
0	The decoder output buffer is not full
1	The decoder output buffer is full

BUSY bit: should be set to “1” during the initialization of the decoder or when the decoder start to work. This bit can be cleared by writing “1”

MP3 Format Register0 (Read $18h : / Write : inhibit)
MP3 Format Register1 (Read $1Ah : / Write : inhibit)
MP3 Format Register2 (Read $1Ch : / Write : inhibit)

MP3 Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$18h		- -	- -	- -	- -	PAD 0	CRC 0	PLY1 0	PLY0 1	MP3 format register0
$1Ah		FRQ3 0	FRQ2 0	FRQ1 0	FRQ0 0	BT3 0	BT2 0	BT1 0	BT0 0	MP3 format register1
$1Ch		EP1 0	EP0 0	ORID 0	CPRT 0	EXM1 0	EXM0 0	MOD1 0	MOD0 0	MP3 format register2

MP3 Format Register0,1,2 is the register used to identify MP3 format. After the mp3 data has been identified by MP3 decoder, the result will be set into these registers. These registers can be used for debugging.

PAD bit: represents the status of the PADDING bit of the mp3 data during decoding.

PAD	Description
0	PADDING bit is 0
1	PADDING bit is 1

CRC bit: represents whether CRC is implemented during the mp3 data decoding.

CRC	Description
0	CRC is not implemented
1	CRC is implemented

PLY1、PLY0 bit: represents the layer number of the mp3 data during decoding.

PLY1	PLY0	Description
0	0	Not used
0	1	LAYER-3
1	0	LAYER-2
1	1	LAYER-1

FRQ3、FRQ2、FRQ1、FRQ0 bit: represents the mp3 data sampling frequency during decoding.

FRQ3	FRQ2	FRQ1	FRQ0	Description
0	0	0	0	8kHz
0	0	0	1	11.025kHz
0	0	1	0	12kHz
0	0	1	1	16kHz
0	1	0	0	22.05kHz
0	1	0	1	24kHz
0	1	1	0	32kHz
0	1	1	1	44.1kHz
1	0	0	0	48kHz

BT3、BT2、BT1、BT0 bit: represents the bit rate of mp3 data during decoding.

BT3	BT2	BT1	BT0	Description	
				MPEG1(kbps)	MPEG2, MPEG2.5(kbps)
0	0	0	0	Free format	Free format
0	0	0	1	32	8
0	0	1	0	40	16
0	0	1	1	48	24
0	1	0	0	56	32
0	1	0	1	64	40
0	1	1	0	80	48
0	1	1	1	96	56
1	0	0	0	112	64
1	0	0	1	128	80
1	0	1	0	160	96
1	0	1	1	192	112
1	1	0	0	224	128
1	1	0	1	256	144
1	1	1	0	320	160
1	1	1	1	Not used	Not used

EP1、EP0 bit: represents the Emphasis mode of mp3 file during decoding.

EP1	EP0	Description
0	0	No emphasis
0	1	50/15ms
1	0	Not used
1	1	CCITT J.17

ORID bit: represents the mp3 file in decoding is original or copied.

ORID	Description
0	Original
1	Copied

CPRT bit: represents whether the mp3 file in decoding has copyright.

CPRT	Description
0	No copyright
1	Has copyright

EXM1、EXM0 bit: represents the extension mode of the mp3 data in decoding.

EXM1	EXM0	Description
0	0	No extension
0	1	Intensity stereo
1	0	Mid-side stereo
1	1	intensity stereo&mid-side stereo

MOD1、MOD0 bit: represents the channel mode of the mp3 file in decoding.

MOD1	MOD0	Description
0	0	Stereo
0	1	Joint Stereo
1	0	Dual Channel
1	1	Monaural

MP3 Data Request Select (Read : $1Eh / Write : $1Fh)

MP3 Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$1Eh	$1Fh	-	-	-	-	-	-	-	DRQSEL	MP3Data Request Select
		-	-	-	-	-	-	-	0	

MP3 data request mode configuration register.

DRQSEL bit: configure mp3 data request mode.

DRQSEL	Description
0	DREQ&FIFO EMPTY mode
1	FIFO Threshold mode

DREQ&FIFO EMPTY mode:
Use MP3 data request register and FIFO status register, and to generate the data request interrupt through data request signal of internal MP3 decoder or EMPTY status of MP3 FIFO.

FIFO Threshold mode：
Generate data request interrupt by defining the threshold of MP3 FIFO.

Power Down Register(Read $20h : / Write : $21h)

LSI Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$20h	$21h	-	-	-	CLPD	CLKE	-	-	-	Power Down
		-	-	-	0	0	-	-	-	

This register used to setup power down of the different modules of the LSI. These bits are allocated to different modules, and used as power down signal.

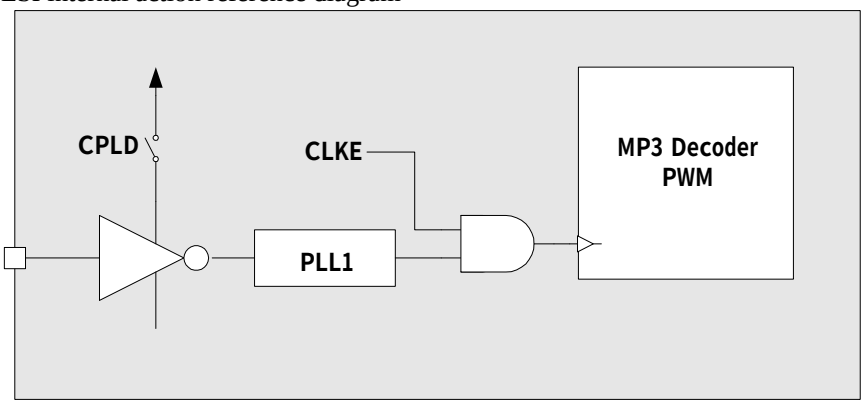
CLKE bit: Stop supplying clock to MP3 decoder and PWM module.

CLKE	Description
0	Stop supplying clock to MP3 decoder and PWM module
1	Supply clock to MP3 decoder and PWM module

CLPD bit: control Oscillation module.

CLPD	Description
0	Release the Power down state of Oscillation module
1	Oscillation module under power down state

LSI internal action reference diagram



Clock Register(Read $22h : / Write : $23h)

LSI Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$22h	$23h	PLL2 0	PLL1 0	PLL0 0	CK4 0	CK3 0	CK2 0	CK1 0	CK0 0	Clock

The clock register determines the MP3 decoder clock as submultiples of the master clock.. CK4-0 bits used to set the division ratio of the master lock to the PLL. The PLL then multiplies that clock by the times which is corresponded to PLL bits. MP3 decoder clock is half of PLL clock, thus generating the MP3 decoder clock that should range between 15 and 20MHz.
PLL2-0 bits indicate the multiplication of clock by PLL operation.

Value (CK4-0)	Divided Ratio	Value (CK4-0)	Divided Ratio
00H	1	0AH	11
01H	2	0BH	12
02H	3	0CH	13
03H	4	0DH	14
04H	5	0EH	15
05H	6	0FH	16
06H	7	10H	17
07H	8	11H	18
08H	9	12H	19
09H	10	13H	20
		14H-1FH	N/A

Value (PLL2-0)	Times by PLL	Value (PLL2-0)	Times by PLL
0h	Inhibit (Not use PLL)	4h	16
1h	10	5h	18
2h	12	6h	20
3h	14	7h	20

PLL2 Clock Division Register(Read $24h : / Write : $25h)

LSI Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$24h	$25h	- -	- -	PL2DIV5 0	PL2DIV4 0	PL2DIV3 0	PL2DIV2 0	PL2DIV1 0	PL2DIV0 0	PLL2 Clock Division

This register indicates the division ratio of master clock to the PLL2 clock. Please setup the division ratio and note that the PLL2 clock should range between 1MHz and 4MHz.

For the clock that have been divided by the division ratio set in this register, it will be multipled by PLL2 at half of the multiple ratio as defined in the 64KMUL,88KMUL,96KMUL registers. The multipled clock will be divided by 64KDIV，88KDIV, 96KDIV, and the clock after division should be 64*64K, 64*88.2K, 64*96K respectively.

During system initialization, please configure the following registers by the master clock in use. When mp3 music is played, mp3 decoder will automatically select the most optimum value for different registers according to the actual sampling rate of the different mp3 music.
Clock register, PLL2 Clock Division Register
64K Audio Clock Division Register, 64K Audio Clock Multiple Register
88K Audio Clock Division Register, 88K Audio Clock Multiple Register
96K Audio Clock Division Register, 96K Audio Clock Multiple Register

Please calculate the values for the different registers using OKI Clock Claculator tool.

64K Audio Clock Division Register(Read $26h : / Write : $27h)

LSI Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$26h	$27h	- -	- -	64DIV5 0	64DIV4 0	64DIV3 0	64DIV2 0	64DIV1 0	64DIV0 0	64K Audio Clock Division

This register will set the division ratio when the MP3 sampling frequency is 32kHz series (8, 16, 32 kHz) and at 64FS.

Please set this register during initialization when power on. Please use OKI Clock Calculator tool to calculate the setting value.

64K Audio Clock Multiple Register(Read $28h : / Write : $29h)

LSI Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$28h	$29h	- -	64MUL6 0	64MUL5 0	64MUL4 0	64MUL3 0	64MUL2 0	64MUL1 0	64MUL0 0	64K Audio Clock Multiple

This register will set the multiple ratio when the MP3 sampling frequency is 32kHz series (8, 16, 32 kHz) and at 64FS.

Please set this register during initialization when power on. Please use OKI Clock Calculator tool to calculate the setting value.

Value 64MUL<6:0>	Times by PLL2	Value 64MUL<6:0>	Times by PLL2
00h-13h	Inhibit	1Eh	15.0
14h	10.0	1Fh	15.5
15h	10.5	20h	16.0
16h	11.0	21h	16.5
17h	11.5	22h	17.0
18h	12.0	23h	17.5
19h	12.5	24h	18.0
1Ah	13.0	25h	18.5
1Bh	13.5	26h	19.0
1Ch	14.0	27h	19.5
1Dh	14.5	28h	20.0
		29h-7Fh	Inhibit

88K Audio Clock Division Register(Read $2Ah : / Write : $2Bh)

LSI Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$2Ah	$2Bh	-	-	88DIV5	88DIV4	88DIV3	88DIV2	88DIV1	88DIV0	88K Audio Clock
		-	-	0	0	0	0	0	0	Division

This register will set the division ratio when the MP3 sampling frequency is 44.1kHz series (11.025K, 22.05K, 44.1K) and at 88FS.

Please set this register during initialization when power on. Please use OKI Clock Calculator tool to calculate the setting value.

88K Audio Clock Multiple Register(Read $2Ch : / Write : $2Dh)

LSI Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$2Ch	$2Dh	-	88MUL6	88MUL5	88MUL4	88MUL3	88MUL2	88MUL1	88MUL0	88K Audio Clock
		-	0	0	0	0	0	0	0	Multiple

This register will set the multiple ratio when the MP3 sampling frequency is 44.1kHz series (11.025K, 22.05K, 44.1K) and at 88FS.

Please set this register during initialization when power on. Please use OKI Clock Calculator tool to calculate the setting value.

Value 88MUL<6:0>	Times by PLL2	Value 88MUL<6:0>	Times by PLL2
00h-13h	Inhibit	1Eh	15.0
14h	10.0	1Fh	15.5
15h	10.5	20h	16.0
16h	11.0	21h	16.5
17h	11.5	22h	17.0
18h	12.0	23h	17.5
19h	12.5	24h	18.0
1Ah	13.0	25h	18.5
1Bh	13.5	26h	19.0
1Ch	14.0	27h	19.5
1Dh	14.5	28h	20.0
		29h-7Fh	Inhibit

96K Audio Clock Division Register(Read $2Eh : / Write : $2Fh)

LSI Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$2Eh	$2Fh	-	-	96DIV5	96DIV4	96DIV3	96DIV2	96DIV1	96DIV0	96K Audio Clock
		-	-	0	0	0	0	0	0	Division

This register will set the division ratio when the MP3 sampling frequency is 48kHz series (12K, 24K, 48K) and at 96FS.

Please set this register during initialization when power on. Please use OKI Clock Calculator tool to calculate the setting value.

96K Audio Clock Multiple Register(Read $30h : / Write : $31h)

LSI Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$30h	$31h	- -	96MUL6 0	96MUL5 0	96MUL4 0	96MUL3 0	96MUL2 0	96MUL1 0	96MUL0 0	96K Audio Clock Multiple

This register will set the multiple ratio when the MP3 sampling frequency is 48kHz series (12K, 24K, 48K) and at 96FS.

Please set this register during initialization when power on. Please use OKI Clock Calculator tool to calculate the setting value.

Value 96MUL<6:0>	Times by PLL2	Value 96MUL<6:0>	Times by PLL2
00h-13h	Inhibit	1Eh	15.0
14h	10.0	1Fh	15.5
15h	10.5	20h	16.0
16h	11.0	21h	16.5
17h	11.5	22h	17.0
18h	12.0	23h	17.5
19h	12.5	24h	18.0
1Ah	13.0	25h	18.5
1Bh	13.5	26h	19.0
1Ch	14.0	27h	19.5
1Dh	14.5	28h	20.0
		29h-7Fh	Inhibit

External Clock Control Register(Read $32h : / Write : $33h)

LSI Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$32h	$33h	FEED 0	- -	- -	- -	- -	- -	- -	- -	Ext CLK Control

This register used to define the ON/OFF of the feedback resistor in the clock port. When the input clock is small amplitude signal, FEED bit must be set as “1”.

FEED bit: used to define the ON/OFF of the feedback resistor in the clock port

FEED	Description
0	Feedback resistor OFF
1	Feedback resistor ON

Soft Reset Register (Read $34h / Write : $35h)

LSI Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$34h	$35h	-	-	-	-	-	-	-	SRST	Soft Reset
		-	-	-	-	-	-	-	0	

This register is used to initialize all the modules of LSI. (Except for some setup values of registers). For those need to be reset, please refer to "REGISTER AND FUNCTION STATUS AFTER RESET, SOFT RESET, DURING POWERDOWN AND AFTER CLEARING POWER DOWN".

If the SRST bit of soft reset register is set to "1", it is in reset status. If SRST bit is set to "0", reset status will be released.

NOTICE: When internal CLK stopped (CLK=0), and it is in Power down status (CLKE=0, CLPD=0), the soft reset can not be used. Please use it in normal working status (CLKE=1, CLPD=0).

Interrupt Enable Register(Read $38h : / Write : $39h)

Interrupt Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$38h	$39h	ISS 0	PLKE 0	ENDE 0	FRME 0	WARNE 0	ERRE 0	DRQE 0	MONE 0	Interrupt Enable

This register is used for setting the enability for interrupt request.

ISS bit: Polarity switch of IRQ pin

ISS	Description
0	IRQ pin enable at high level
1	IRQ pin enable at low level

PLKE bit: Enable/Disenable PLL2 LOCK stop interrupt signal

PLKE	Description
0	Disenable PLL2 LOCK stop interrupt
1	Enable PLL2 LOCK stop interrupt

ENDE bit: Enable/Disenable MP3 stop playing interrupt

ENDE	Description
0	Disenable MP3 stop playing interrupt
1	Enable MP3 stop playing interrupt

FRME bit: Enable/Disenable MP3 synchronized word interrupt

FRME	Description
0	Disenable MP3 synchronized word interrupt
1	Enable MP3 synchronized word interrupt

WARNE bit: Enable/Disenable MP3 warning interrupt

WARNE	Description
0	Disenable MP3 warning interrupt
1	Enable MP3 warning interrupt

ERRE bit：Enable/Disenable MP3 error interrupt

ERRE	Description
0	Disenable MP3 error interrupt
1	Enable MP3 error interrupt

DRQE bit：Enable/Disenable MP3 data request interrput

DRQE	Description
0	Disenable MP3 data request interrput
1	Enable MP3 data request interrput

MONE bit：Enable/Disenable MP3 stop data playing interrput

MONE	Description
0	Disenable MP3 stop data playing interrput
1	Enable MP3 stop data playing interrput

Interrupt Request Register(Read $3Ah : / Write : $3Bh)

Interrupt Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$2Ch	$2Dh	-	PLK	ENDST	FRMST	WARNST	ERRST	FIFODRQST	MONST	Interrupt Request
		-	0	0	0	0	0	1	0	

This register outputs different kinds of interrupt. Interrupt request outputs interrupt signal from IRQ pin. If there is interrupt signal occurred from IRQ pin, please confirm the different status through this register.

PLK bit: It is set to “1” when PLL2 LOCK finished. After MP3 decoder detects the synchronized word of MP3 data, PLL2 is started. When PLL2 LOCK finished, it is set to “1”. This bit can be cleared by writing “1”.

PLK	Description
0	PLL2 Lock not be finished
1	PLL2 Lock be finished

ENDST bit: It is set to “1” when MP3 music playback finished. When the decoded PCM data stopped, and MP3 FIFO is also empty. This bit will be set to “1”. This bit can be cleared by writing “1”.

ENDST	Description
0	During playing or stand by
1	Playing finished

FRMST bit: When the MP3 decoder detects the synchronized word, this bit will be set to “1”. This bit can be cleared by writing “1”.

FRMST	Description
0	MP3 decoder did not detect the synchronized word
1	MP3 decoder detected the synchronized word

WARNST bit: This bit will be set to “1” when MP3 decoder generates warning signal. Please confirm the warning cause by check the MP3WarningRegister. This bit can be cleared by clearing MP3WarningRegister.

WARNST	Description
0	MP3 decoder didn’t generate warning signal
1	MP3 decoder generated warning signal

ERRST bit: This bit will be set to “1” when MP3 data error occurred. Please confirm the error cause by check the MP3ErrorRegister. This bit can be cleared by clearing MP3ErrorRegister.

ERRST	Description
1	MP3 data error didn’t occur
0	MP3 data error occurred

FIFODRQST bit: According to the setting of the MP3 data request select register, the condition which data request will be occurred is also different.

MP3DRQ mode：Data request signal will be generated by internal MP3 decoder, or the Empty status of MP3FIFO will generate interrupt signal. When the interrupt signal is generated by data request signal of internal MP3 decoder, this bit can be cleared by writing "1". When the interrupt signal is generated by the Empty status of MP3 FIFO, this bit can be cleared by writing data to FIFO.

FIFOST mode： FIFO Threshold mode. To clear this bit, more amount of data than the threshold need to be written into FIFO.

FIFODRQST	Description
0	No data request needed
1	Data request needed

MONST bit: This bit will be set to "1" when MP3 playing is stopped forcibly. And this bit can be cleared by writing "1".

MONST	Description
0	MP3 is playing
1	MP3 play stopped

Port IO Register(Read $42h : / Write : $43h)

Port Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(initial)								
$42h	$43h	- -	- -	PIO5 0	- -	- -	- -	- -	PIO0 0	Port IO

Port IO register decides whether a GPIO pin is output or input.

When the corresponding bit in the Port IO register is “0”, the assigned port is an input port. When the corresponding bit in the Port IO register is “1”, the assigned port is an output port.

Port Register(Read $44h : / Write : $45h)

Port Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(initial)								
$44h	$45h	- -	- -	P5 ?	- -	- -	- -	- -	P0 ?	Port

When PORT IO register is “1”, the value in PORT register is output to PORT pin.
When PORT IO register is “0”, the value of PORT pin can be read from the corresponding bit of PORT register.

PWMA Register(Read $48h : / Write : $49h)
VIB Register(Read $52h : / Write : $53h)

Port Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$48h	$49h	WAE 0	WA6 0	WA5 0	WA4 0	WA3 0	WA2 0	WA1 0	WA0 0	PWMA
$52h	$53h	WVE 0	WV6 0	WV5 0	WV4 0	WV3 0	WV2 0	WV1 0	WV0 0	VIB

PWMA and Vib register is to adjust duty ratio of each PWM output from P0 pin and P5 pin.

Duty ratio can implenment the 128 steps adjustment from 0 to 127, according to the lower 7bits setting , such as WA6-WA0. On the other side, MSB of the register is enable or disable of PWM output. When MSB is “1”, PWM will be outputted. When MSB is “0”, PWM does not output any signal.

Pull Up Register (Read $54h : / Write : $55h)

Port Control Register										
INDEX		b07	b06	B05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$54h	$55h	-	-	PUP5	-	-	-	-	PUP0	Pull up(Port)
		-	-	1	-	-	-	-	1	

PULL UP register is enabled or disabled pull up register on each PORT pin.

When the bit is “0”, pull-up resistor is connected on an assigned pin. When the bit is “1” pull-up resistor is not connected on the pin.

PWM Output Select Register(Read $56h : / Write : $57h)

Port Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$56h	$57h	-	-	P5M	-	-	-	-	P0M	PWM output select
		-	-	0	-	-	-	-	0	

This register is to select wether the port is used for GPIO port or PWM output port.

When the bit value of the register is “0”, the port defined by this bit is used for GPIO port. When the bit value of the register is “1”, the port defined by this bit is used for PWM output port. It is possible to control the different ports independently. When the port is used for driving LED, please refer to BLOCK DIAGRAM.

Port Enable Register(Read $58h : / Write : $59h)

Port Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$58h	$59h	-	-	P5E	-	-	-	-	P0E	Port Enable
		-	-	1	-	-	-	-	1	

“Port Enable” register specify the port is enabling or disenabling.

When bit value in the register is “1”, the status of port which is defined by this bit, also depends on “Pull-up” register. When “Pull-up” register is off, the pin is state in Hi-Z. When “pull-up” register is on, the port is connected to pull-up register.
On the other hand, when the port enable register is “L”, the status of port which is defined by this bit, also depends on “Port register”, “Port IO” register, and “Pull-up” register.

“Port IO” register, and “Pull-up” register.

PORT Enable Register	Pull-up register	Port state
L	-	Depend on “Port” register, “Port IO” register, “Pull-up” register.
H	L	Pull-up
H	H	Hi-Z

Audio Volume Register(Read $62h : / Write : $63h)

Analog Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$62h	$63h	HPV3 0	HPV2 1	HPV1 0	HPV0 0	AV3 0	AV2 1	AV1 0	AV0 0	Audio Volume

Audio Volume register is to control volume of audio output.
Lower 4bit is for output from AOUT pin, and upper 4bit is from LOUT and ROUT. It should be used for volume control for terminal device.

AV3-0 HPV3-0	Volume	AV3-0 HPV3-0	Volume
0x00	12.0dB	0x08	-12.0dB
0x01	9.5dB	0x09	-14.5dB
0x02	6.0dB	0x0A	-18.1dB
0x03	3.5dB	0x0B	-20.6dB
0x04	0.0dB	0x0C	-24.1dB
0x05	-2.5dB	0x0D	-26.6dB
0x06	-6.0dB	0x0E	-30.1dB
0x07	-8.5dB	0x0F	MUTE

AV3-0 bit: change volume for AOUT pin.
HPV3-0 bit: change volume for LOUT and ROUT pin.

SP Volume Register (Read $64h : / Write : $65h)

Analog Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$64h	$65h	-	-	-	-	SPV3	SPV2	SPV1	SPV0	SP volume t
		-	-	-	-	0	0	0	0	

This register is to adjust the volume of Speaker Amp.

Please refer to the following table for the setting.

SPV3-0	Gain[dB]	SPV3-0	Gain[dB]
0x00h	7	0x08h	-9.1
0x01h	5.1	0x09h	-11.2
0x02h	3	0x0Ah	-13.3
0x03h	1.1	0x0Bh	-15.4
0x04h	-0.9	0x0Ch	-17.5
0x05h	-2.9	0x0Dh	-19.6
0x06h	-4.9	0x0Eh	-21.8
0x07h	-7	0x0Fh	MUTE

HP Power Down Register(Read $66h : / Write : $67h)

Analog Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$66h	$67h	BIASL 0	PDL 1	ENR2L 1	ENL2L 1	BIASR 0	PDR 1	ENL2R 1	ENR2R 1	HP Power Down

HP Power Down register specifies enabling or disenabling power down of headphone amplifier. The detail is shown below.

Output			Analog power down Register							
ROUT	LOUT	note	BIASR	PDR	ENL2R	ENR2R	BIASL	PDL	ENR2L	ENL2L
Rch	Lch	Stereo	?	0	0	1	?	0	0	1
Lch + Rch	Lch + Rch	mix	?	0	1	1	?	0	1	1
(No use)	Lch + Rch	monaural	?	1	*	*	?	0	1	1
Lch + Rch	(No use)	monaural	?	0	1	1	?	1	*	*
Lch	Rch	opposite	?	0	1	0	?	0	1	0
(No use)	(No Use)	Power Down	?	1	*	*	?	1	*	*
(DC)	(DC)	Inhibition	?	0	0	0	?	0	0	0

Lch = L output is enable, Rch = R output is enable, ? = depending on system, * = don't care

NOTICE
It is prohibited to use both signal from LOUT/ROUT pin and AOUT pin as a same time.

BIASR: Select enabling or disenabling voltage bias to reduce pop noise when reset and set power down of ROUT pin.
BIASR = 0 : Bias register for ROUT is DISENABLE.
BIASR = 1 : Bias register for ROUT is ENABLE.

PDR: Select enabling or disenabling audio output from ROUT pin.
PDR = 0 : ROUT is ENABLE.
PDR = 1 : ROUT is DISENABLE

ENR2R: Enable output of right audio output from ROUT pin.
ENR2R=0: Disenable
ENR2R=1: Enable

ENL2R: Enable output of left audio output from ROUT pin.
ENL2R=0: Disenable
ENL2R=1: Enable

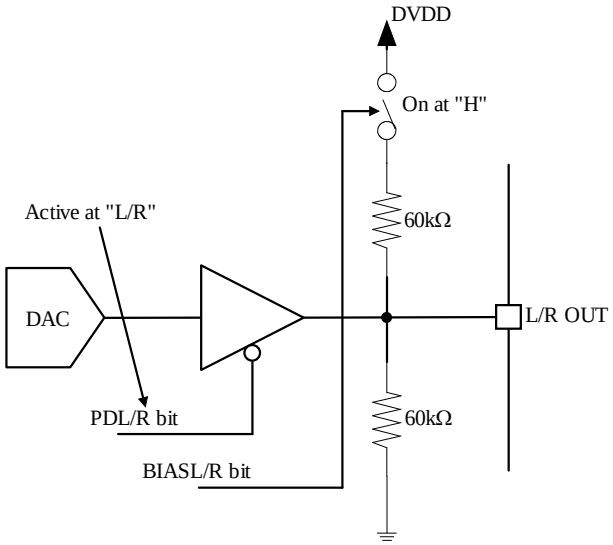
BIASL: Select enabling or disenabling voltage bias to reduce pop noise when reset and set power down of LOUT pin.
BIASL = 0 : Bias register for LOUT is DISENABLE.
BIASL = 1 : Bias register for LOUT is ENABLE.

PDL: Select enabling or disenabling audio output from LOUT pin.
PDL = 0 : LOUT is ENABLE.
PDL = 1 : LOUT is DISENABLE.

ENL2L: Enable output of left audio output from LOUT pin.

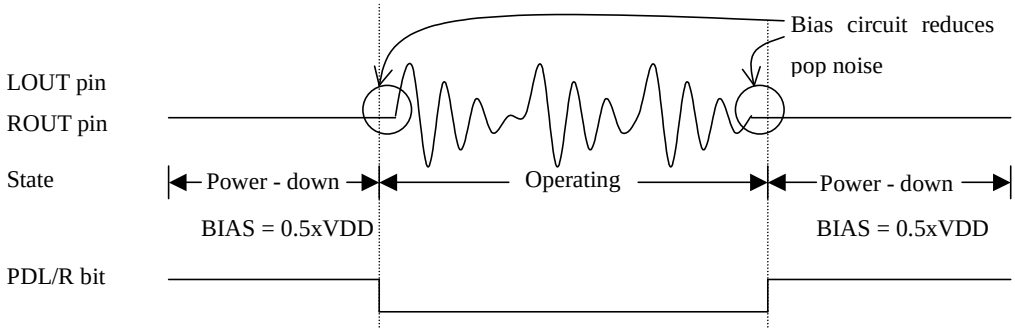
ENR2L: Enable output of right audio output from LOUT pin.

The LSI includes following circuit for reducing pop noise.



Please refer to the figures below for the difference analog level of BIASL/R bit.

<BIASL/R bit = 1>

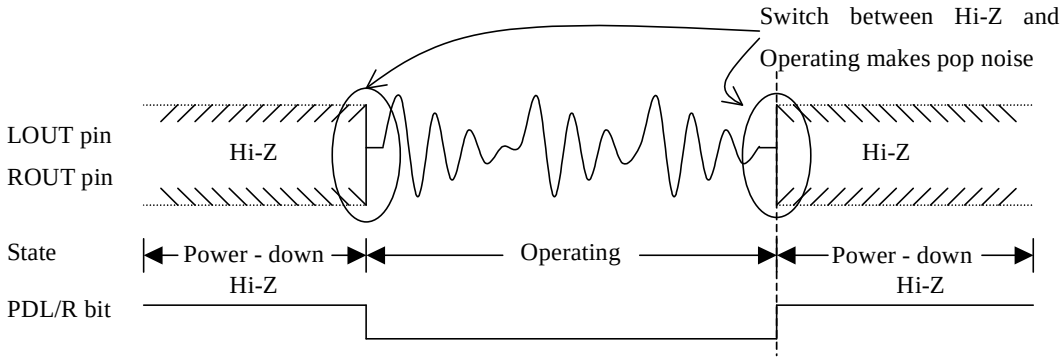


The voltage of LOUT and ROUT pin under Hi-Z status is set to proper value during operating. It reduces pop noise when switch between Hi-Z mode and Operating mode.

During power-down mode, the voltage of LOUT and ROUT pin is set approximately as the operating value. So the "pop" noise can be reduced when switch between Power-down mode and Operating mode.

NOTE : BIAS circuit can NOT delete pop noise completely. Please make sure that it's in tolerance level.

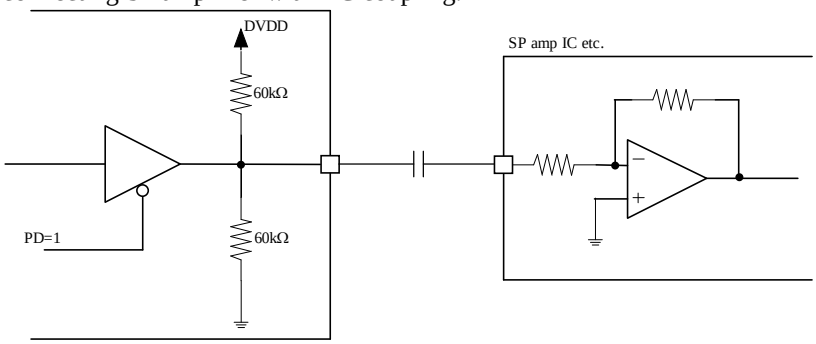
<BIASL/R bit = 0>



Because the voltage of LOUT and ROUT pin is indeterminate in Hi-Z, switch between Hi-Z status and Operating status makes major pop noise.

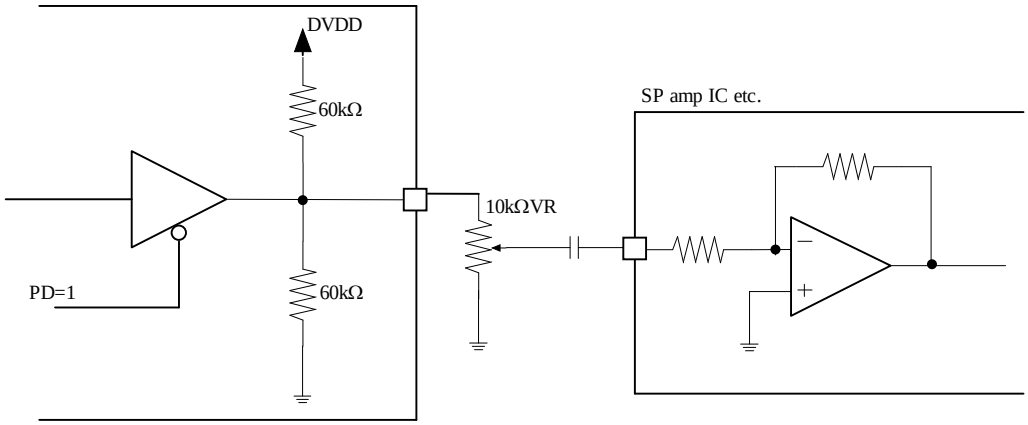
Speaker amplifier should be connected to the LSI as follows.

Recommended circuit = connecting SP amplifier with AC coupling.



BIAS Level is set about 0.5 x Vpp

NOTE: In the case of following circuit, the BIAS circuit for reducing pop noise doesn't work properly. Therefore set the BIASL/R bit = 0, and reduce pop noise by adding external circuit.



HP Out Invert Register(Read $68h : / Write : $69h)

Analog Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$68h	$69h	- -	- -	- -	- -	- -	- -	AORINV 0	AOLINV 0	HP Out Invert (for BTL mode)

HPOUT Invert register specifies the phase of analog output from LOUT and ROUT pins.

When the register is set to BTL output, PSRR can be improved more than 6dB. BTL Output mode can be configured by the setting below.

- AORINV bit = 1, AOLINV bit = 0
- all bit of ENL2R,ENR2R,ENR2L,ENL2L in “HP Power Down” register is set to “H”.
- Set same value to left channel and right channel in “Audio Volume” register

AOLINV: Select the phase with LOUT-pin. When the AOLINV=1 are selected, the phase of analog signal outputted form LOUT-pin is inverted.
AORINV: Select the phase with ROUT-pin. When the AORINV=1 are selected, the phase of analog signal outputted form ROUT-pin is inverted.

Analog Power Down Register(Read $6Ah : / Write : $6Bh)

Analog Control Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$6Ah	$6Bh	- -	- -	- -	- -	- -	- -	MOE_N 1	SPE_N 1	Analog Power Down (APD)

MOE_N bit enables/disables AOUT to output audio signal. When this bit is “0”, from DAC to AOUT is enabled, and MIXIN and MIXOUT are also enabled. When the bit is “1”, AOUT output , MIXIN and MIXOUT is in power down state.

SPE_N bit enables/disables the output of speaker amplifier. When the bit is”0”, speaker amplifier is enabled. When the bit is “1”, the amplifier is in power down state.

NOTICE
It is prohibited to use both signal from LOUT/ROUT pin and AOUT pin as the same time.

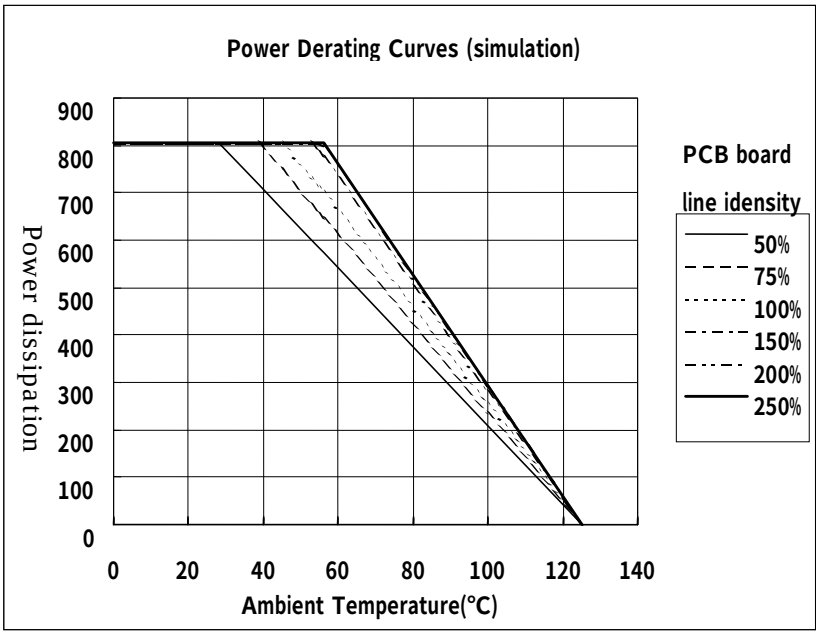
Product ID Register(Read $F0h : / Write : inhibit)

Product Identification Register										
INDEX		b07	b06	b05	b04	b03	b02	b01	b00	NOTE
R	W	(Initial)								
$F0h		D7	D6	D5	D4	D3	D2	**D1**	D0	Product ID
		1	0	0	0	0	**0**	0	0	

Every product is assigned to a specific product ID.

Product Name	Product ID
ML2873	0x03
ML2871	0x04
ML2863	0x05
ML2872	0x14
ML2865	0x15
ML2011	0x80

Power Derating Curves (Pdmax=805mW)(TBD)



Ambient Temperature in Degrees C
Pdmax=805mW,for 4.5V,W
Package: P-VQFN32-0506-0.50
Base board size: 70mm×35mm×1.0mm
Base board matching line density diagram.
Base board matching line density is showed in the following table.

- PCB board

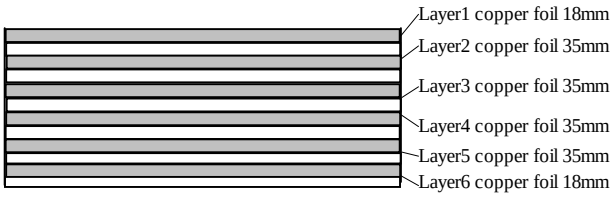
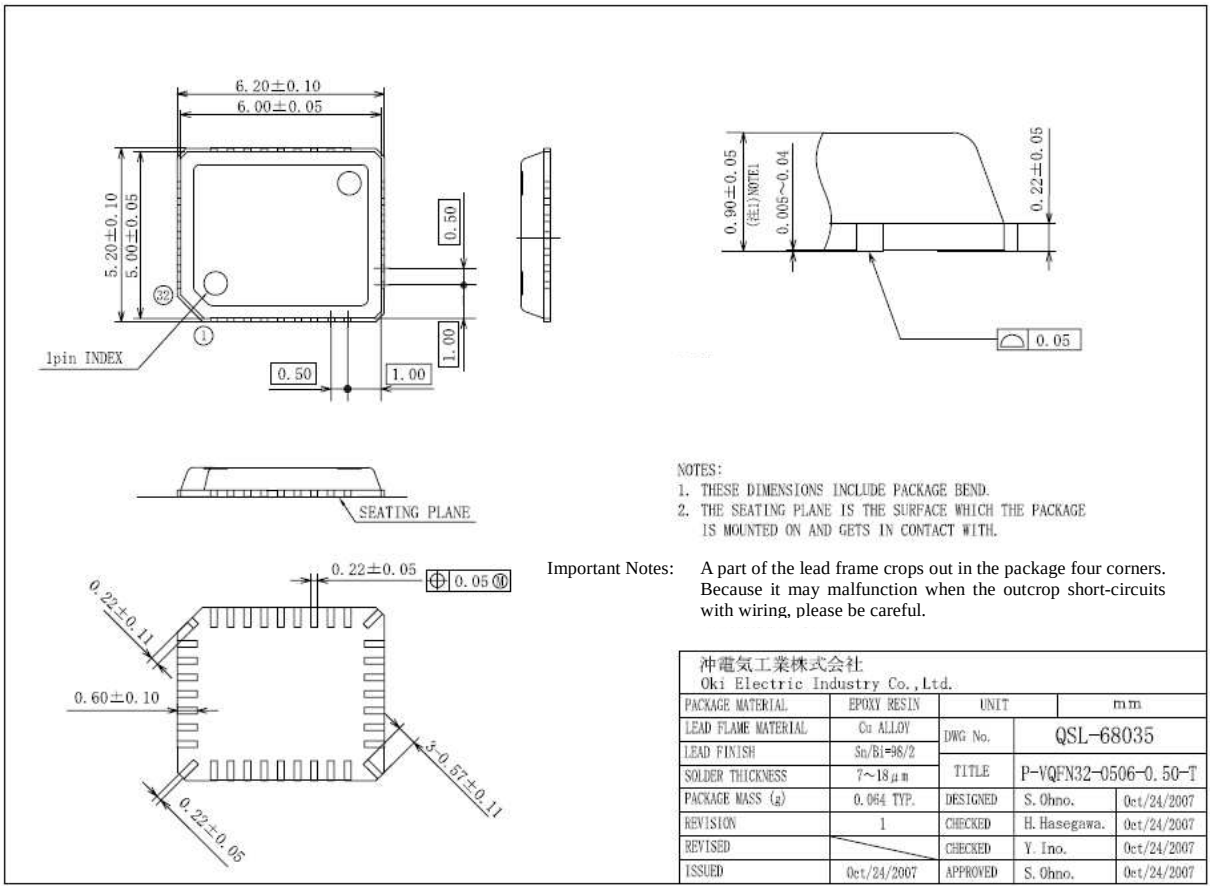


Table 1

Simulation Result	Simulation Condition						
qja(°C /W)	PCB board line density	Layer 1	Layer 2	Layer 3	Layer 4	Layer 5	Layer 6
120.0	50%	50%	-	-	-	-	-
106.6	75%	75%	-	-	-	-	-
98.6	100%	50%	50%	-	-	-	-
89.0	150%	50%	100%	-	-	-	-
86.3	200%	50%	100%	50%	-	-	-
84.9	250%	50%	100%	100%	-	-	-

Package dimensions

32PIN QFN

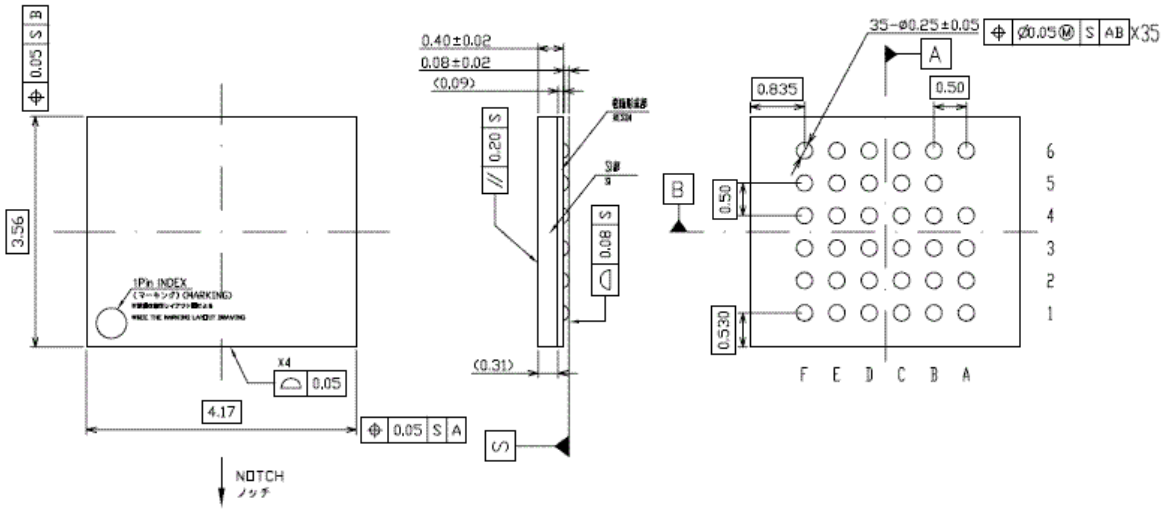


NOTES:
1. THESE DIMENSIONS INCLUDE PACKAGE BEND.
2. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

Important Notes: A part of the lead frame crops out in the package four corners. Because it may malfunction when the outcrop short-circuits with wiring, please be careful.

沖電気工業株式会社 Oki Electric Industry Co.,Ltd.			
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FRAME MATERIAL	Cu ALLOY	DWG No.	QSL-68035
LEAD FINISH	Sn/Bi=96/2		
SOLDER THICKNESS	7~18μm	TITLE	P-VQFN32-0506-0.50-T
PACKAGE MASS (g)	0.064 TYP.	DESIGNED	S. Ohno. Oct/24/2007
REVISION	1	CHECKED	H. Hasegawa. Oct/24/2007
REVISED		CHECKED	Y. Ino. Oct/24/2007
ISSUED	Oct/24/2007	APPROVED	S. Ohno. Oct/24/2007

35PIN WCSP



注記：
1．端子ピッチは端子中央部の位置で規定する。
2．AP工程管理寸法項目は「AP工程設計書」、出荷検査項目は「検査仕様書」による。

ATTENTION
1. THE TERMINAL PITCH MEANS THE DISTANCES BETWEEN THE TERMINAL CENTERS.
2. THE DIMENSION ITEMS CONTROLLED ASSEMBLY PROCESS APPLIES CORRESPONDINGLY (AP PROCESS DESIGN) AND THE ITEMS OF FINAL INSPECTION APPLIES CORRESPONDINGLY (INSPECTION SPECIFICATION)

Revision history

Date	Page	Notes	Revision
06.03.24	All	Preliminary version release	1.0.0
06.03.28	8	Modified the pin name	1.0.1
07.01.26	All	Remove “confidential” and “Preliminary”.	1.0.2
07.07.06	16	DC Characteristics VIH2 and VIL2	1.0.3
07.07.06	82	Package Dimensions	1.0.3
07.09.19	All	Final version release	2
07.11.20	4	Add Design Support Tools	3
07.11.20	75	Change 32pin QFN Package Dimensions	3

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.
2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.
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4. Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters beyond the specified maximum ratings or operation outside the specified operating range.
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   Such applications include, but are not limited to, traffic and automotive equipment, safety devices, aerospace equipment, nuclear power control, medical equipment, and life-support systems.
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