ML2841 Data Sheet

Preliminary Version 1.0.4
Revised on 12 March 2007

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Contents

ML2841 DATA SHEET

Low power MP3 decoder, SRS 3D, 64polyphinic ringtone

Version1.0.3, Revised on Monday, March 12, 2007

1 General Description

1.1 General Description

ML2841 is low power and high quality MP3 playback and 64poly ringtone with 3D surround. The MP3 decoder consists of hard-wired technology. Therefore, playback term of MP3 file shall be longer. Besides, the LSI has 3D surround by SRS Labs who is leading company for 3D surround.

1.2 Features

- Sound Generator
  - High quality PCM sound generator
  - Support General MIDI
  - Maximum 64 polyphony simultaneously

- MP3 decoder
  - Low power MP3 decoder (power consumption of core = typ 5mW)
  - Supported format: MPEG1/2/2.5 audio layer III
  - Supported mode: Mono, Stereo, Dual, Joint-stereo(I-stereo, M/S-stereo)
  - Ultimate low power consumption
  - Possible to play sound generator simultaneously
  - Recognize and skip ID3-Tag Ver 1.0, 2.2, 2.3, 2.4

- ADPCM/PCM decoder
  - Supported format: OKI 2bit and 4bit ADPCM, 8bit and 16bit PCM
  - Sampling frequency: 4.0/5.3/6.4/8.0/10.6/12.8/16.0/32.0kHz

- CPU I/F
  - 8bit parallel I/F, 3 or 4 wired SPI selectable

- Serial Audio Interface Tranceiver/Receiver
  - Sampling frequency: 8.0/11.025/12.0/16.0/22.05/24.0/32.0/44.1/48.0kHz
  - Bit length: fixed 16bit
  - Support master mode

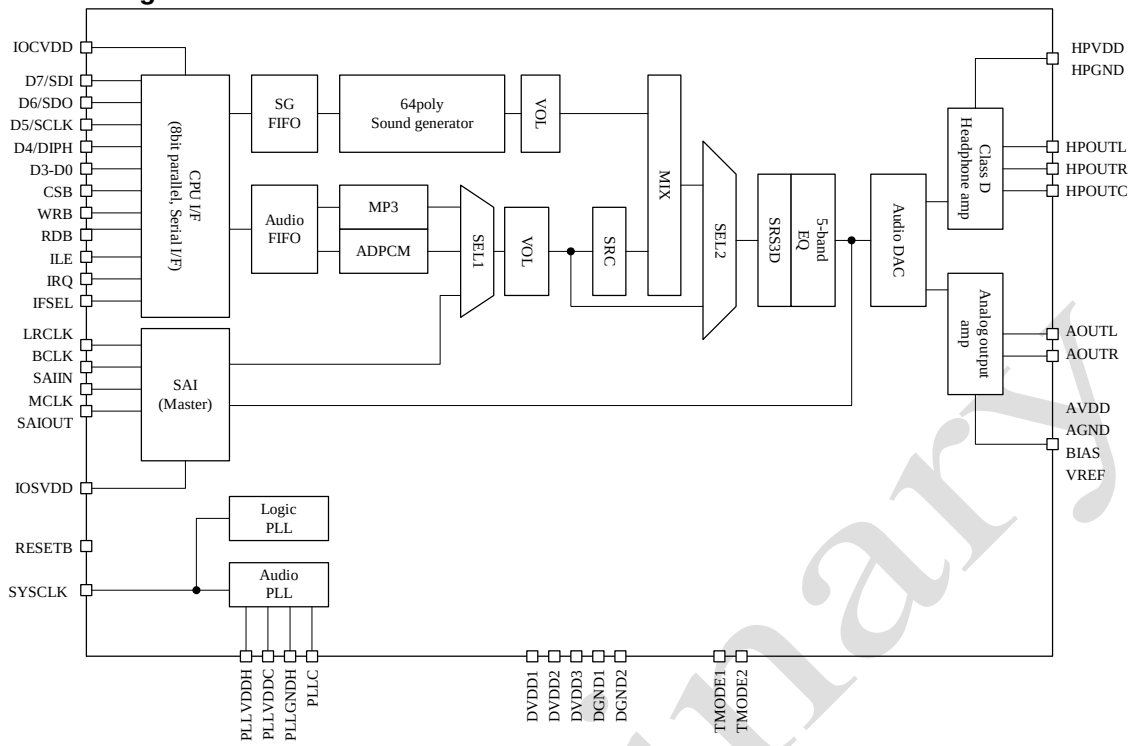
- 3D surround
  - High quality 3D surround SRS3D by SRS Labs
  - Support two kinds of 3D surround:
    SRS3D extreme mode: 3D surround for near two speaker
    SRS3D headphone: 3D surround for headphone
  - Ultimate low power consumption of 3D surround : 0.3mW by 3D surround
- 5-band Equalizer
  - Hardwired 5-band Equalizer for low power consumption

- Stereo audio DAC
  - 16bit stereo audio DAC

- Audio output
  - Stereo analog output
  - Stereo headphone amplifier by Class D for low power consumption

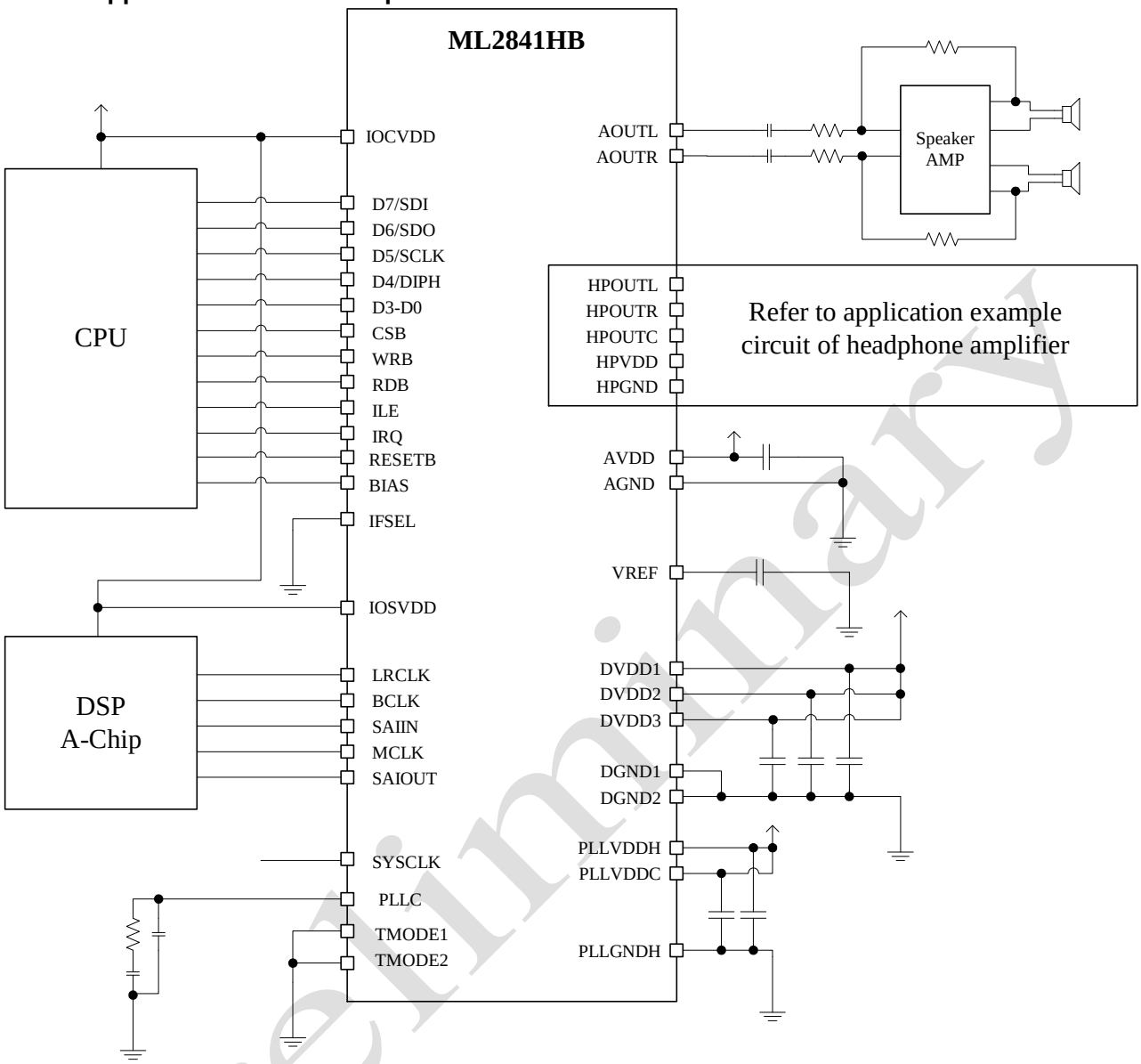
- Package
  - 49pin 0.5mm pitch W-CSP

1.3 Block Diagram

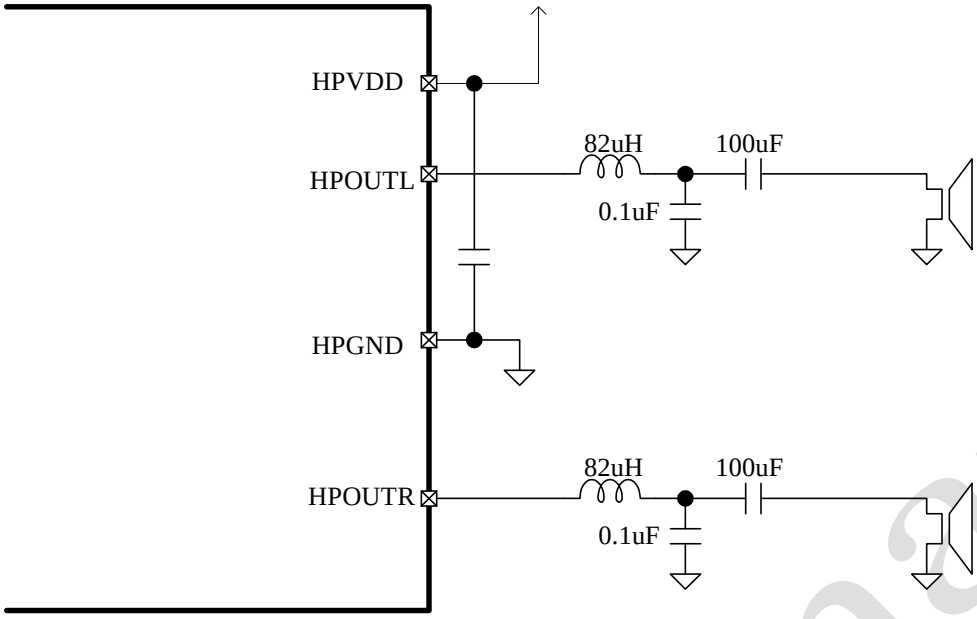


Explanation of block diagram
SAI (Master): Serial Audio Interface for external audio. The block supports master mode.
Audio FIFO: FIFO for ADPCM and MP3. Either of ADPCM or MP3 can be in use.
SG FIFO: FIFO for sound generator
SRC: Sampling Rate Converter for mixing between sound generator and other audio source.
SRS3D: 3D surround by SRS Labs
VOL: Volume
MIX: Mixing block
SEL1: Selector of MP3, ADPCM or External Audio input from SAIR.
SEL2: select bypass or mixed sound

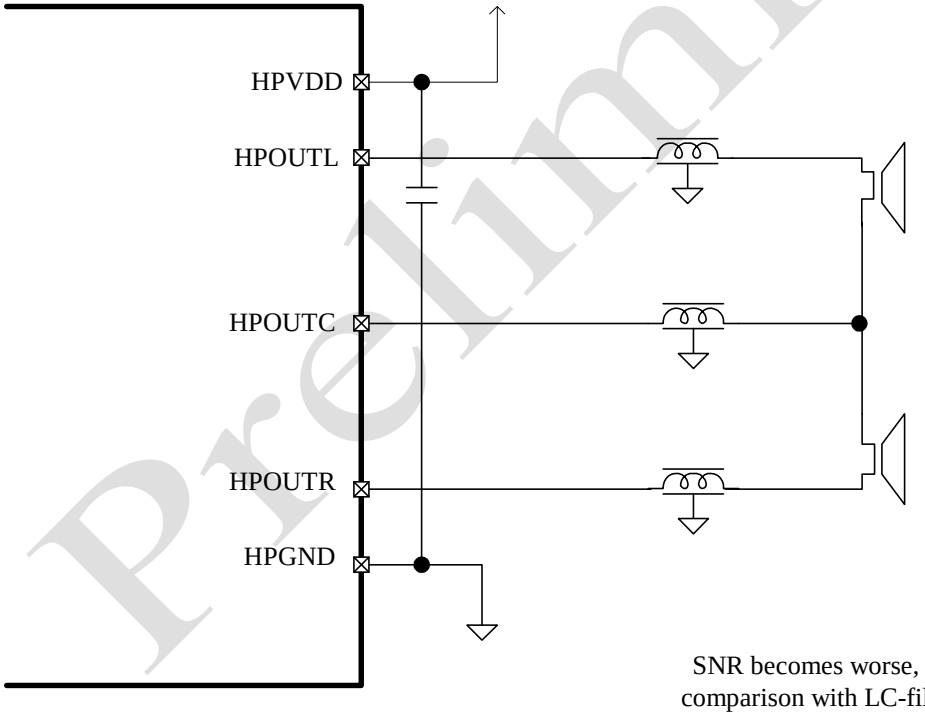
1.4 Application Circuit Examples



1.4.1 Application Circuit Example of Headphone amplifier I



1.4.2 Application Circuit Examples of headphone amplifier II (Non DC cut capacitor)



SNR becomes worse, in comparison with LC-filter

1.5 Pin Description

1.5.1 Pin List

Pin No	8bit Parallel	Dir	Pin No	SPI	Dir	Memo
D6	D7	IO	D6	SDI	I	
D7	D6	IO	D7	SDO	O	
D5	D5	IO	D5	SCLK	I	
C5	D4	IO	C5	DIPH	I	
B6	D3	IO		-	-	
A6	D2	IO		-	-	
B5	D1	IO		-	-	
A5	D0	IO		-	-	
C4	CSB	I	C4	CSB	I	
B4	RDB	I		-	-	
A4	WRB	I		-	-	
D4	ILE	I		-	-	
E7	IRQ	O	E7	IRQ	O	
E5	ISS	I	E5	ISS	I	
E6	IFSEL	I	E6	IFSEL	I	
E3	LRCLK	IO	E3	LRCLK	IO	
F1	BCLK	IO	F1	BCLK	IO	
E2	SAIIN	I	E2	SAIIN	I	
E1	MCLK	IO	E1	MCLK	IO	
F2	RESETB	I	F2	RESETB	I	Noise filter
C1	SYSCLK	I	C1	SYSCLK	I	
G7	TMODE0	I	G7	TMODE0	I	Pull-Down
A1	TMODE1	I	A1	TMODE1	I	Pull-Down
F7	HPOUTR	O	F7	HPOUTR	O	
F5	HPOUTL	O	F5	HPOUTL	O	
F6	HPOUTC	O	F6	HPOUTC	O	
G4	AOUTR	O	G4	AOUTR	O	
G3	AOUTL	O	G3	AOUTL	O	
G2	VREF	I	G2	VREF	I	
E4	BIAS	I	E4	BIAS	I	Pull-Down
A2	PLLC	I	A2	PLLC	I	
D3	DVDD	-	D3	DVDD	-	
C3	DVDD	-	C3	DVDD	-	
C7	DVDD	-	C7	DVDD	-	
B1	DVDD	-	B1	DVDD	-	
D1	DGND	-	D1	DGND	-	
A3	DGND	-	A3	DGND	-	
C6	DGND	-	C6	DGND	-	
B7	IOCVDD	-	B7	IOCVDD	-	
D2	IOSVDD	-	D2	IOSVDD	-	
F3	AVDD	-	F3	AVDD	-	
F4	AGND	-	F4	AGND	-	
G5	HPVDD	-	G5	HPVDD	-	
G6	HPGND	-	G6	HPGND	-	
B2	PLLVDDH	-	B2	PLLVDDH	-	
B3	PLLGNDH	-	B3	PLLGNDH	-	
C2	PLLVDDC	-	C2	PLLVDDC	-	
G1	SAIOUT	O	G1	SAIOUT	O	

1.5.2 Pin Description

No	Name	Description	Power supply	Active	Memo
	D7/SDI	When IFSEL is “H”, it is MSB pin of parallel CPU I/F When IFSEL is “L”, it is serial data input pin.	IOCVDD	-	
	D6/SDO	When IFSEL is “H”, it is 2MSB pin of parallel CPU I/F When IFSEL is “L”, it is serial data output pin.	IOCVDD	-	
	D5/SCLK	When IFSEL is “H”, it is 3MSB pin of parallel CPU I/F When IFSEL is “L”, it is serial data clock pin.	IOCVDD	-	
	D4/DIPH	When IFSEL is “H”, it is 4MSB pin of parallel CPU I/F When IFSEL is “L”, it is to select serial clock timing.	IOCVDD	-	
	D3	5MSB pin of parallel CPU I/F	IOCVDD	-	
	D2	6MSB pin of parallel CPU I/F	IOCVDD	-	
	D1	7MSB pin of parallel CPU I/F	IOCVDD	-	
	D0	LSB pin of parallel CPU I/F	IOCVDD	-	
	CSB	Chip enable pin	IOCVDD	L	
	RDB	Read enable pin for parallel CPU I/F	IOCVDD	L	
	WRB	Write enable pin for parallel CPU I/F	IOCVDD	L	
	ILE	Index select signal for parallel CPU I/F. When ILE =”H”, Data from D7-0 pins is INDEX. When ILE =”L”, Data from D7-0 pins is data.	IOCVDD	H	
	IRQ	Interrupt Request pin	IOCVDD	-	
	ISS	select IRQ signal level. When ISS=”H”, IRQ is low-active. When ISS=”L”, IRQ is high-active.	IOCVDD	-	
	IFSEL	Interface Select Signal H:8bit-Parallel, L: Serial Interface	IOCVDD	-	
	BCLK	BLCK of SAI	IOSVDD	-	
	LRCLK	LRCLK of SAI	IOSVDD	-	
	SAIIN	Serial data input of SAI	IOSVDD	-	
	MCLK	Audio 256fs clock pin for SAI	IOSVDD	-	
	RESETB	Reset LSI. When RESETB=”L”, LSI is reset, and possible to turn DVDD off for saving power consumption.	IOSVDD	L	
	SYSCLK	System clockinput Possible to input 12, 13, 13.5, 14.4, 15.36, 16, 19.2, 19.68, 19.8, 26, 27MHz	IOSVDD	-	
	TMODE0	TEST pin. It must be fixed as “L”.	IOCVDD	H	
	TMODE1	TEST pin. It must be fixed as “L”.	IOSVDD	H	
	HPOUTL	Left channel of headphone output	HPVDD	-	
	HPOUTR	Right channel of headphone output	HPVDD	-	
	HPOUTC	Common output for headphone amplifier	HPVDD	-	
	AOUTL	Left channel of audio output	AVDD	-	
	AOUTR	Right channel of audio output	AVDD	-	
	BIAS	It enables or disables to force bias to AOUTL, AOUTR and, VREF. L: AOUTL, AOUTR and VREF pins will be Hi-Z. H: enables bias.	IOSVDD	H	BIAS pin set to "H" or PDANA bit and PDDAC bit of OUTCNT register set to "1" to enable to force bias to AOUTL, AOUTR and, VREF.
	VREF	Analog Reference voltage output pin. Please connect 1μF capacitor near by the pin.	AVDD	-	
	PLLC	Audio PLL loop filter pin. Please connect CR filter near by the pin.	DVDD	-	
	DVDD	VDDpin for core block please insert 1.5V.	-	-	
	DGND	GND pin for core block.	-	-	
	IOCVDD	VDD pin for IO block. Please insert 1.65~3.6V.	-	-	
	IOSVDD	VDD pin for SAI block. Please insert 1.65~3.6V.	-	-	
	AVDD	Analog VDD pin. Please insert 3.3V	-	-	
	AGND	Analog GND pin	-	-	
	HPVDD	VDD pin for headphone amplifier. Please insert 3.3V.	-	-	
	HPGND	GND pin for headphone amplifier.		-	For HPOUTR, HPOUTL and

					HPOUTC.
	PLLVDDH	VDD pin for audio PLL. Please insert 3.3V		-	
	PLLGNDH	GND pin for audio PLL.		-	
	PLLVDDC	VDD pin for audio PLL. Please insert 3.3V.		-	
	SAIOUT	Serial Audio Interface PCM Output pin	IOSVDD	-	

1.5.3 Pin Layout

TMODE0	HPOUTR	IRQ	D6	DVDD	IOCVDD	NC	7
HPGND	HPOUTC	IFSEL	D7	DGND	D3	D2	6
HPVDD	HPOUTL	ISS	D5	D4	D1	D0	5
AOUTR	AGND	BIAS	ILE	CSB	RDB	WRB	4
AOUTL	AVDD	LRCLK	DVDD	DVDD	PLLGNDH	DGND	3
VREF	RESETB	SAIIN	IOSVDD	PLLVDDC	PLLVDDH	PLLC	2
SAIOUT	BCLK	MCLK	DGND	SYSCLK	DVDD	TMODE1	1
G	F	E	D	C	B	A	

Bottom view

INDEX

1.6 Register map

1.6.1 Clock Register

Address	Register name	Symbol	R/W	Default
0x0000	Input Clock Setting register	SYSFRQ	R/W	0x00
0x0010	Audio PLL Times Setting register 1	APLLTIME1	R/W	0x00
0x0012	Audio PLL Times Setting register 0	APLLTIME0	R/W	0x00
0x0014	Audio PLL Division register 1	APLLDIV1	R/W	0x00
0x0016	Audio PLL Division register 0	APLLDIV0	R/W	0x00
0x0018	Audio PLL VCO setting register	APLLP	R/W	0x00
0x001A	Audio PLL Mode register	APLLFC	R/W	0x00
0x001C	Audio PLL Enable register	APLLEN	R/W	0x00
0x0020	Logic PLL Times register	LPLLTIME	R/W	0x00
0x0022	Logic PLL Division register	LPLLDIV	R/W	0x00
0x0024	Logic PLL Enable register	LPLLEN	R/W	0x00
0x0040	Software Reset register	SRST	R/W	0x00

1.6.2 Host-IF Register

Address	Register name	Symbol	R/W	Default
0x**FE	Upper Address Setting register	HADDR	R/W	0x00

1.6.3 SG Register

Address	Register name	Symbol	R/W	Default
0x0100	SG FIFO register	SGFIFO	W	-
0x0102	SG FIFO Threshold register	SGFIFOT	R/W	0x00
0x0106	SG FIFO Clear register	SGFIFOCLR	W	-
0x0108	SG FIFO Status register	SGFIFOST	R	0x03
0x010A	SG Control register	SGCNT	R/W	0x00
0x010C	Sync Play Enable register	SYNCPLAY	R/W	0x00
0x010E	Relative Tempo Setting register	RTEMPO	R/W	0x00
0x0110	Transpose Setting register	TPOSE	R/W	0x00
0x0112	Current Time Setting register	CTCNT	R/W	0x00
0x0114	Current Time register 0	CTIME0	R	0x00
0x0116	Current Time register 1	CTIME1	R	0x00
0x0118	Current Time register 2	CTIME2	R	0x00
0x011A	Current Time register 3	CTIME3	R	0x00
0x011C	LED Synchronization register 0	LED0	R	0x00
0x011E	LED Synchronization register 1	LED1	R	0x00
0x0120	LED Synchronization register 2	LED2	R	0x00
0x0122	LED Synchronization register 3	LED3	R	0x00
0x0124	VIB Synchronization register	VIB	R	0x00
0x0126	Sync Count register	SYNCC	R	0x00
0x0128	SG Sync Status register	SGsyncst	R/W	0x00

1.6.4 MP3 Register

Address	Register name	Symbol	R/W	Default
0x0200	MP3 FIFO register	MP3FIFO	W	-
0x0202	MP3 FIFO Threshold register 0	MP3FIFOT0	R/W	0x00
0x0204	MP3 FIFO Threshold register 1	MP3FIFOT1	R/W	0x00
0x0206	MP3 FIFO Clear register	MP3FIFOCLR	W	-
0x0208	MP3 FIFO Status register	MP3FIFOST	R	0x03
0x020A	MP3 Control register	MP3CNT	R/W	0x00
0x020C	MP3 Dual Channel Select register	MP3CHSEL	R/W	0x00
0x0210	MP3 FIFO Request Number register 1	MP3FIFON1	R	0xFF
0x0212	MP3 Error register	MP3ERR	R/W	0x00
0x0216	MP3 Status register	MP3STAT	R/W	0x01
0x0218	MP3 Interrupt Mode register	MP3DRQSEL	R/W	0x00

1.6.5 ADPCM Register

Address	Register name	Symbol	R/W	Default
0x0300	ADPCM FIFO register	ADFIFO	W	-
0x0302	ADPCM FIFO Threshold register 0	ADFIFOT0	R/W	0x00
0x0304	ADPCM FIFO Threshold register 1	ADFIFOT1	R/W	0x00
0x0306	ADPCM FIFO Clear register	ADFIFOCLR	W	-
0x0308	ADPCM Status Clear register	ADFIFOST	R	0x03
0x030A	ADPCM Control register 0	ADPCNT0	R/W	0x00
0x030C	ADPCM Control register 1	ADPCNT1	R/W	0x00

1.6.6 SAI Register

Address	Register name	Symbol	R/W	Default
0x0400	SAI Control register 0	SAICON0	R/W	0x00
0x0402	SAI Control register 1	SAICON1	R/W	0x01
0x0404	SAI Sampling Frequency register	SAIFRQ	R/W	0x00
0x0406	SAI Control register 2	SAICON2	R/W	0x00

1.6.7 SRC Register

Address	Register name	Symbol	R/W	Default
0x0500	Playback Select register	MIXSEL	R/W	0x00
0x0502	SG Volume register	SGVOL	R/W	0x00
0x0504	SG Balance register	SGBAL	R/W	0x00
0x0506	SRC Volume register	SRCVOL	R/W	0x00
0x0508	SRC Balance register	SRCBAL	R/W	0x00
0x050A	POP Noise Filter Control register	POPCNT	R/W	0x00

1.6.8 3D Surround register

Address	Register name	Symbol	R/W	Default
0x0600	SRS3D Enable register	SRS3DEN	R/W	0x00
0x0602	SRS3D Mode register	SRS3DMODE	R/W	0x00
0x0604	SRS3D Control register	SRS3DSWCNT	R/W	0x66
0x0606	SRS3D Extreme Control register	SRS3DEWCNT	R/W	0x66

1.6.9 Equalizer Register

Address	Register name	Symbol	R/W	Default
0x0700	EQ Enable register	EQEN	R/W	0x00
0x0702	EQ Band 0 Gain register	EQGAIN0	R/W	0x0A
0x0704	EQ Band 1 Gain register	EQGAIN1	R/W	0x0A
0x0706	EQ Band 2 Gain register	EQGAIN2	R/W	0x0A
0x0708	EQ Band 3 Gain register	EQGAIN3	R/W	0x0A
0x070A	EQ Band 4 Gain register	EQGAIN4	R/W	0x0A

1.6.10 DAC and Headphone Amplifier register

Address	Register name	Symbol	R/W	Default
0x0800	Output Control register	OUTCNT	R/W	0x00
0x0802	Headphone Setting register	HPMOD	R/W	0x04
0x0804	Audio Output Setting register	ANAMOD	R/W	0x05
0x0806	DAC Volume register	DACLVL	R/W	0x00
0x0808	DAC Balance register	DACBAL	R/W	0x00
0x080A	DAC Mute register	DACMUTE	R/W	0x03
0x080C	DAC Volume Adjusting Time register	DACVOLST	R/W	0x01
0x080E	Output Status register	OUTSTAT	R/W	0x00

1.6.11 Interrupt register

Address	Register name	Symbol	R/W	Default
0x0900	Interrupt Module register	IRQMOD	R	0x1C
0x0902	Analog Interrupt register	ANAIRQST	R/W	0x00
0x0904	SAI Interrupt register	SAIIRQST	R/W	0x00
0x0906	ADPCM Interrupt register	ADPIRQST	R/W	0x02
0x0908	MP3 Interrupt register	MP3IRQST	R/W	0x02
0x090A	SG Interrupt register	SGIRQST	R/W	0x02
0x090C	Analog Interrupt Enable register	ANAIRQ	R/W	0x01
0x090E	SAI Interrupt Enable register	SAIIRQ	R/W	0x00
0x0910	ADPCM Interrupt Enable register	ADPIRQ	R/W	0x00
0x0912	MP3 Interrupt Enable register	MP3IRQ	R/W	0x00
0x0914	SG Interrupt Enable register	SGIRQ	R/W	0x00

2 Electric Characteristics

2.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
VDD for CORE block	DVDD	-	-0.3~2.0	V
VDD for IO block	IOCVDD IOSVDD	-	-0.3~4.6	V
VDD for analog block	AVDD	-	-0.3~4.6	V
VDD for headphone amplifiers	HPVDD	-	-0.3~4.6	V
VDD for PLL	PLLVDDH PLLVDDC	-	-0.3~4.6	V
Input Voltage	VI	-	-0.3~IOCVDD+0.3 -0.3~IOSVDD+0.3	V
Output Current	Io	-	-16~+16	mA
Power dissipation	Pd	Ta=85°C	700	mW
Storage Temperature	Tstg	-	-65~+150	°C

2.2 Recommended Operating Ranges

Parameter	Symbol	Condition	Operating Range Min	Typ	Max	Unit
VDD for core	DVDD	-	1.35	-	1.65	V
VDD for IO	IOCVDD IOSVDD	-	1.65	-	3.6	V
VDD for analog	AVDD	AVDD≥IOCVDD, IOSVDD AVDD=PLLVDDH, PLLVDDC	2.375	-	3.6	V
VDD for PLL	PLLVDDH PLLVDDC	PLLVDDH, PLLVDDC≥IOSVDD PLLVDDH, PLLVDD= AVDD	2.375	-	3.6	V
VDD for headphone	HPVDD	HPVDD≥IOSVDD	1.6	-	3.6	V
Operating temperature	Top	-	-20	-	85	°C

2.3 DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Applied pin
H input voltage	VIH	DGND=0V	IOCVDD*0.8 IOSVDD*0.8	-	IOCVDD+0.3 IOSVDD+0.3	V	
L input voltage	VIL	DGND=0V	-0.3	-	IOCVDD*0.2 IOSVDD*0.2	V	
H output voltage	VOH	IOH=-135µA	IOCVDD*0.8 IOSVDD*0.8	-	-	V	
L output voltage	VOL	IOL=135µA	-	-	IOCVDD*0.2 IOSVDD*0.2	V	

Input leakage current 1	IL1	VI=IOCVDD, DGND VI=IOSVDD, DGND	-10	-	10	µA	*1
Input leakage current 2	IL2	VI=IOCVDD, DGND VI=IOSVDD, DGND	2	-	200	µA	*2
Current consumption1(Operating)	IDDO	*3	-	10	-	mA	
		*4	-	27	-	mW	
Current consumption2(Operating)	IDDO	*5	-	-	35	mA	
Stanby Current	IDDS	*6	-	1	10	uA	

*1 apply to normal buffer
*2 apply to TMODE0, TMODE1, BIAS pin
*3 DVDD, MP3 playback in bypass mode, headphone amp, no sound, DVDD=1.5V, Ta = 25°C
*4 DVDD+HPVDD+AVDD+PLLVDDC+PLLVDDH+IOCVDD+IOSVDD, Same condition of *3
*5 DVDD-IDDO, MP3+SG+WOW+EQ playback, headphone amp, no sound. Ta = 25°C
*6 DVDD-OFF, HPVDD+AVDD+PLLVDDC+PLLVDDH+IOCVDD+IOSVDD, Ta=25°C

2.4 DAC Characteristics

2.4.1 Class D amplifier

Ta=25°C, HPVDD=3.3V, Headphone amp output load=32Ω ,f=1kHz
Audio sampling frequency = 48 kHz

Parameter	Condition	Min	Typ	Max	Unit
Output power	RL=32Ω	-	10	-	mW
DR	Output level = -60dB A-weight filter Connect LC-filter with HPOUTL and HPOUTR	-	90	-	dB
SNR	Output level = BPZ A-weight filter Connect LC-filter with HPOUTL and HPOUTR.	-	90	-	dB
SNR	Output level = BPZ A-Weight filter Without LC-filter	-	90	-	dB
Headphone Output load		16	-	32	Ω

2.4.2 Analog amplifier Characteristics

Ta=25°C, AVDD=3.3V, f=1kHz
Audio sampling frequency = 48 kHz

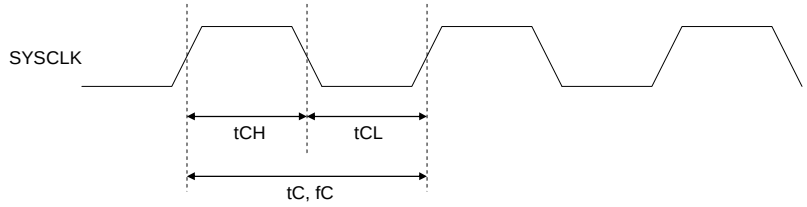
Item	Symbol	Condition	Min	Typ	Max	Unit
Output load	Rload		7	-	-	kΩ
Maximum Output frequency	Fmax	Load=7kΩ	20	-	-	kHz
S/N	SN	Load=7kΩ	-	90	-	dB
PSRR LOW	PSRR	f=217Hz, Output level=BPZ, 200mVpp	-	-60	-	dB
PSRR HIGH	PSRR	f=10kHz, Output level=BPZ, 200mVpp	-	-40	-	dB
Full Scale Range of AOUT	VAOUT		-	0.8*AVDD	-	V
Output Voltage of VREF	VREFO		-	0.5*AVDD	-	V

2.5 AC Characteristics

2.5.1 Clock

DVDD=1.35-1.65V, AVDD=PLLVDDC=PLLVDDH=2.375V-3.6V,
HPVDD=1.65V-3.6V, IOCVDD=IOSVDD=1.65-3.6V, Ta=-20-85°C, CL=30pF

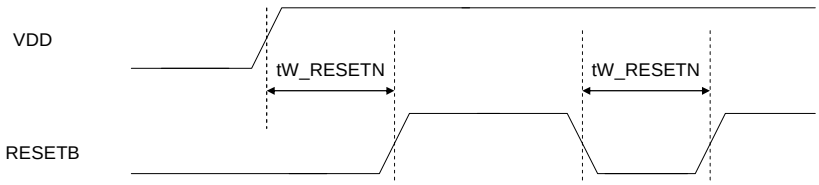
Parameter	Symbol	Min	Max.	Unit
CLOCK frequency	fC	5	30	MHz
CLOCK cycle time	tC	1/fC	1/fC	ns
width of CLOCK high	tCH	12	-	ns
width of CLOCK low	tCL	12	-	ns



2.5.2 RESET

DVDD=1.35-1.65V, AVDD=PLLVDDC=PLLVDDH=2.375V-3.6V,
HPVDD=1.65V-3.6V, IOCVDD=IOSVDD=1.65-3.6V, Ta=-20-85°C, CL=30pF

Parameter	Symbol	Min	Max.	Unit
RESETBPulse width	tW_RST	5	-	µs

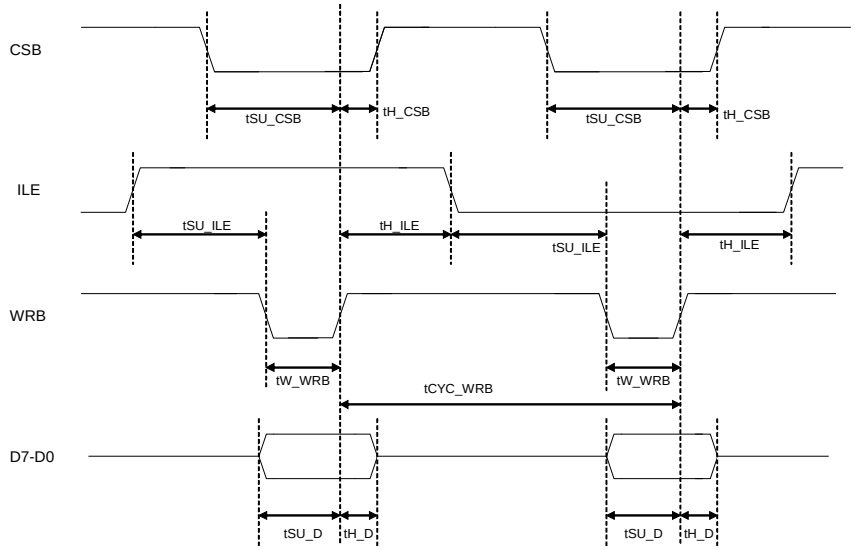


2.5.3 8bit Parallel Interface

DVDD=1.35-1.65V, AVDD=PLLVDDC=PLLVDDH=2.375V-3.6V,
HPVDD=1.65V-3.6V, IOCVDD=IOSVDD=1.65-3.6V, Ta=-20-85°C, CL=30pF

Parameter	Symbol	Min	Max.	Unit
CSB setup time	tSU_CSB	50	-	ns
CSB hold time	tH_CSB	0	-	ns
ILE setup time	tSU_ILE	0	-	ns
ILE hold time	tH_ILE	0	-	ns
Data setup time	tSU_D	50	-	ns
Data hold time	tH_D	0	-	ns
WRB low pulse width	tW_WRB	25	-	ns
Cycle time of WRB	tCYC_WRB	110	-	ns

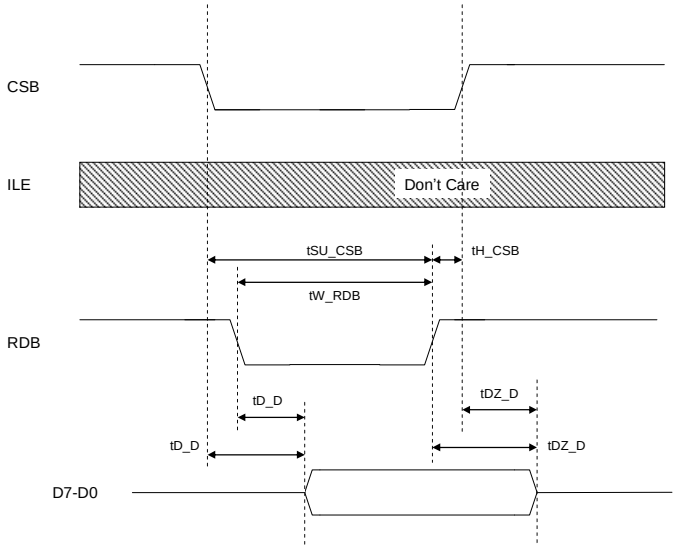
In the case of tW_CSB > tW_WRB:



8bit-Parallel Write Waveform

DVDD=1.35-1.65V, AVDD=PLLVDDC=PLLVDDH=2.375V-3.6V,
HPVDD=1.65V-3.6V, IOCVDD=IOSVDD=1.65-3.6V, Ta=-20-85°C, CL=30pF

Parameter	Symbol	Min	Max.	Unit
CSB setup time	tSU_CSB	50	-	ns
CSB hold time	tH_CSB	0	-	ns
RDB Low pulse width	tW_RDB	85	-	ns
Data delay	tD_D	-	70	ns
Data Hi-Z delay	tDZ_D	-	70	ns

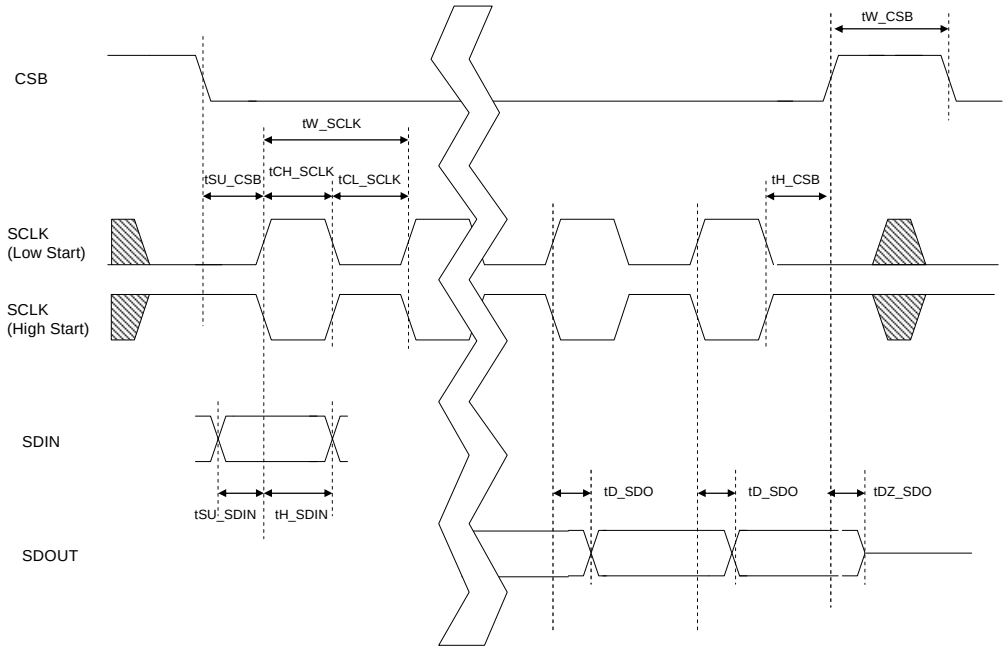


8bit-Parallel Read Waveform

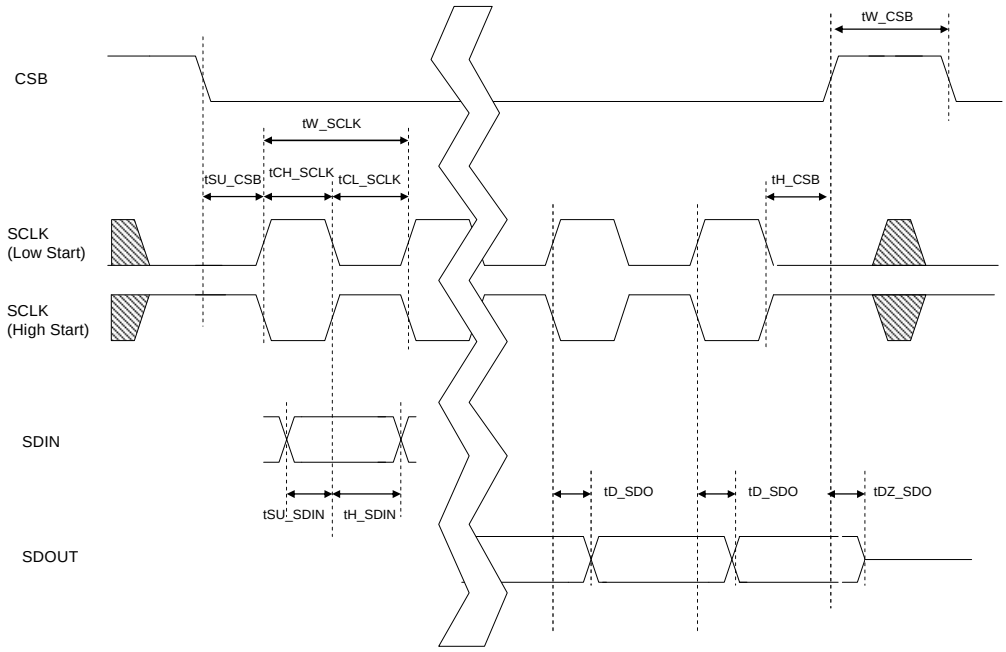
2.5.4 Serial Interface

DVDD=1.35-1.65V, AVDD=PLLVDDC=PLLVDDH=2.375V-3.6V,
HPVDD=1.65V-3.6V, IOCVDD=IOSVDD=1.65-3.6V, Ta=-20-85°C, CL=30pF

Parameter	Symbol	Min	Max.	Unit
width of SCLK low	tCL_SCLK	35	-	ns
width of SCLK high	tCH_SCLK	35	-	ns
SDIN setup time	tSU_SDIN	15	-	ns
SDIN hold time	tH_SDIN	15	-	ns
SDO delay	tD_SDO	25	-	ns
SDO Hi-Z delay	tDZ_SDO	25	-	ns
CSB setup time	tSU_CSB	15	-	ns
CSB hold time	tH_CSB	70	-	ns
width of CSB high	tW_CSB	70	-	ns



SPI AC Waveform (DIPH=1)

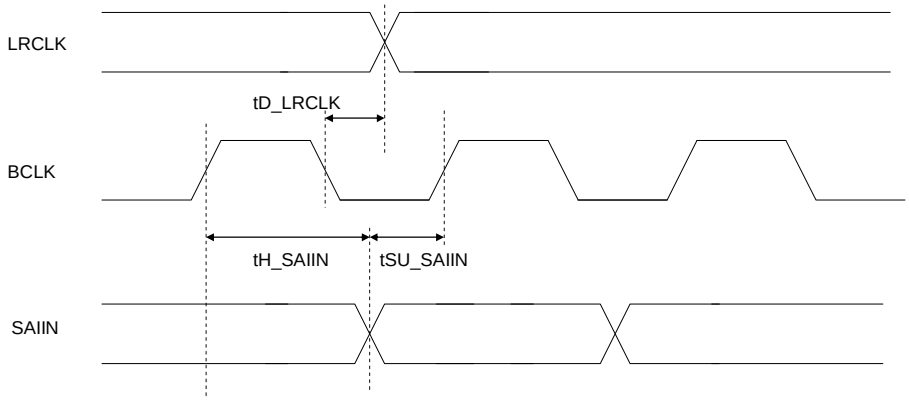


SPI AC Waveform (DIPH=0)

2.5.5 SAIR (Master mode)

DVDD=1.35-1.65V, AVDD=PLLVDDC=PLLVDDH=2.375V-3.6V,
HPVDD=1.65V-3.6V, IOCVDD=IOSVDD=1.65-3.6V, Ta=-20-85°C, CL=30pF

Parameter	Symbol	Min	Max.	Unit
LRCLK output delay	tD_LRCLK	-	70	ns
SAIIN setup time	tSU_SAIIN	60	-	ns
SAIIN hold time	tH_SAIIN	30	-	ns



2.6 Power sequence

Please insert IOCVDD at the beginning in order to avoid conflict of bus signal. Other power supply is optional, when it is unnecessary to use the LSI.
By the same reason, please turn of IOCVDD at last.

3 Register Explanation

3.1 Clock register

3.1.1 Input Clock Setting register (SYSFRQ)

The register is to set parameters related to clock. If following clock in the table below is used, please set AUTOEN bit to "1" and determine clock frequency by SYSFRQ bits.

	7	6	5	4	3	2	1	0
SYSFRQ	AUTOEN	-	-	-	SYSFRQ			
default	0	-	-	-	0	0	0	0

Address: 0x0000
Access: R/W

[Explanation of bit]

- **SYSFRQ**

The bit is to determine system clock frequency. Please set parameters according to following table. When the system clock frequency is supported below, auto setting for detailed parameter can be used. When system clock frequency is not mentioned below, it is unnecessary to set the parameter. In the case, detailed parameter for clock shall be set one by one.

SYSFRQ	System clock frequency (MHz)
0x0	12 (Default)
0x1	13
0x2	13.5
0x3	14.4
0x4	15.36
0x5	16
0x6	19.2
0x7	19.68
0x8	19.8
0x9	26
0xA	27
0xB-0xF	Forbid (same as default)

- **AUTOEN**

The bit is to set enabling or disenabling auto setting for clock.
When system clock is supported in the table above, please set the bit to "1" and set SYSFRQ bits.

AUTOEN	Explanation
0	Manual setting(Default)
1	Auto setting

When AUTOEN bit can be set to "1", following register shall not be changed.
Audio PLL Times Setting register1,0
Audio PLL Division Setting register1, 0
Audio PLL VCO Setting register
Audio PLL Mode register
Logic PLL Times Setting register
Logic PLL Division Setting register
Input Clock Setting register

3.1.2 Audio PLL Times Setting register (APLLTIME1,0)

When LSI supports auto clock setting by "Input Clock Setting register", the register shall not be set. Please ask OKI for detail of the function, when system clock in use is not supported.

7	6	5	4	3	2	1	0

APLLTIME1	-	-	-	-	-	-	APLLTIME1	
default	-	-	-	-	-	-	0	0

Address: 0x0010
Access: R/W

	7	6	5	4	3	2	1	0
APLLTIME0	APLLTIME0							
default	0	0	0	0	0	0	0	0

Address: 0x0012
Access: R/W

3.1.3 Audio PLL Division register (APLLDIV1, 0)

When LSI supports auto clock setting by “Input Clock Setting register”, the register shall not be set. Please ask OKI for detail of the function, when system clock in use is not supported.

	7	6	5	4	3	2	1	0
APLLDIV1	-	-	-	-	-	-	APLLDIV1	
default	-	-	-	-	-	-	0	0

Address: 0x0014
Access: R/W

	7	6	5	4	3	2	1	0
APLLDIV0	APLLDIV0							
default	0	0	0	0	0	0	0	0

Address: 0x0016
Access: R/W

3.1.4 Audio PLL VCO Setting register (APLLP)

When LSI supports auto clock setting by “Input Clock Setting register”, the register shall not be set. Please ask OKI for detail of the function, when system clock in use is not supported.

	7	6	5	4	3	2	1	0
APLLP	-	-	-	-	APLLP			
default	-	-	-	-	0	0	0	0

Address: 0x0018
Access: R/W

3.1.5 Audio PLL Mode register (APLLFC)

When LSI supports auto clock setting by “Input Clock Setting register”, the register shall not be set. Please ask OKI for detail of the function, when system clock in use is not supported.

	7	6	5	4	3	2	1	0
APLLFC	-	-	-	-	-	-	APLLFC	
default	-	-	-	-	-	-	0	0

Address: 0x001A
Access: R/W

APLLFC	VCO frequency
00	40~80MHz
01	20~40MHz
10	10~20MHz
11	Forbid

3.1.6 Audio PLL Enable register (APLLEN)

The register is to stop or start oscillation of Audio PLL.

	7	6	5	4	3	2	1	0
APLLEN	-	-	-	-	-	-	-	APLLEN
default	-	-	-	-	-	-	-	0

Address: 0x001C
Access: R/W

[Explanation of bit]

- **APLLEN**

APLLEN	Explanation
0	Stop oscillation of audio PLL (Default)
1	Start oscillation of audio PLL

3.1.7 Logic PLL Times register (LPLLTIME)

When LSI supports auto clock setting by “Input Clock Setting register”, the register shall not be set. Please ask OKI for detail of the function, when system clock in use is not supported.

	7	6	5	4	3	2	1	0
LPLLTIME	-	-	LPLLTIME					
default	-	-	0	0	0	0	0	0

Address: 0x0020
Access: R/W

3.1.8 Logic PLL Division register (LPLLDIV)

When LSI supports auto clock setting by “Input Clock Setting register”, the register shall not be set. Please ask OKI for detail of the function, when system clock in use is not supported.

	7	6	5	4	3	2	1	0
LPLLDIV	-	-	-	-	-	LPLLDIV		
default	-	-	-	-	-	0	0	0

Address: 0x0022
Access: R/W

3.1.9 Logic PLL Enable register (LPLLEN)

The register is to enable or disenable logic PLL. When logic PLL reactivates after disenable logic PLL, please reset the LSI by hardware reset or software reset.

	7	6	5	4	3	2	1	0
LPLLEN	-	-	-	-	-	-	-	LPLLEN

default	-	-	-	-	-	-	-	0

Address: 0x0024
Access: R/W

LPLLEN	Explanation
0	Disenable logic PLL (Default)
1	Enable logic PLL

3.1.10 Software Reset register (SRST)

The register is to enable or disenable software reset. When write “1” to the register, LSI is reset. In order to release the software reset, please the bit shall be set to "0".

	7	6	5	4	3	2	1	0
SRST	-	-	-	-	-	-	-	SRST
default	-	-	-	-	-	-	-	0

Address: 0x0040
Access: R/W

3.2 Host Interface register

3.2.1 Upper Address Setting register (HADDR)

Address map of ML2841 is 16bits. The register is to set upper byte of address.

	7	6	5	4	3	2	1	0
HADDR	HADDR							
default	0	0	0	0	0	0	0	0

Address: 0x**FE
Access: R/W

NOTICE:
“0” shall be set to upper 4bit.

3.3 Sound Generator register

3.3.1 SG FIFO register(SGFIFO)

The register is FIFO memory for sound generator. Please send MIDI file to the register.

	7	6	5	4	3	2	1	0
SGFIFO	SGFIFO							
default	-	-	-	-	-	-	-	-

address: 0x0100
access: W

3.3.2 SG FIFO Threshold register (SGFIFOT)

This register is to set threshold of SGFIFO for interrupt request. When remain of SGFIFO is the register and below, the request output interrupt request for SGFIFO.

	7	6	5	4	3	2	1	0
SGFIFOT	SGFIFOT							
default	0	0	0	0	0	0	0	0

address: 0x0102
access: R/W

3.3.3 Sound Generator FIFO Clear register (SGFIFOCLR)

The register is to clear SGFIFO. Before start playback by sound generator, please clear SGFIFO by the bit. When the bit is set to "1", SGFIFO is cleared.

	7	6	5	4	3	2	1	0
SGFIFOCLR	-	-	-	-	-	-	-	SGFIFOCLR
default	-	-	-	-	-	-	-	-

address: 0x0106
access: W

3.3.4 Sound Generator FIFO Status register (SGFIFOST)

The register describes sound generator FIFO status.

	7	6	5	4	3	2	1	0
SGFIFOST	-	-	-	-	-	SGFFULL	SGFTHR	SGFEMPTY
default	-	-	-	-	-	0	1	1

address: 0x0108
access: R
[explanation of bit]

- **SGFEMPTY**

When the bit is “1”, SGFIFO is empty.

- **SGFTHR**

When the bit is “1”, number of data in SGFIFO is threshold of SGFIFO by “SGFIFOT register” and the below. Same bit is output in “Interrupt request register”.

- **SGFFULL**

When the bit is “1”, FIFO is full. When any data is written to SGFIFO that is full, data is abandoned.

3.3.5 Sound Generator Control register (SGCNT)

The register is to start playback or to pause of sound generator.

	7	6	5	4	3	2	1	0
SGCNT	-	-	-	-	-	-	SGPAUSE	SGSTART
default	-	-	-	-	-	-	0	0

address: 0x010A
access: R/W
[explanation of bit]

- **SGSTART**

The bit is to start or stop playback of sound generator. When the bit is set from "0" to "1", LSI starts playback. When the bit is set from "1" to "0", LSI stops playback.

SGSTART	Explanation
0	Stop playback of sound generator (Default)
1	Start playback of sound generator

- **SGPAUSE**

The bit is to set or to release pause playback of sound generator.

SGPAUSE	Explanation
0	Not pause (Default)
1	Pause

3.3.6 Sync Play Enable register (SYNCPLAY)

The register is to synchronize sound generator with ADPCM or MP3. When the bit is set to "1", the synchronization is available. ADPCM and MP3 playback will start by trigger from sound generator when recognize CUE message in MIDI file.

	7	6	5	4	3	2	1	0
SYNCPLAY	-	-	-	-	-	-	-	SYNCPLAY
default	-	-	-	-	-	-	-	0

address: 0x010C
access: R/W

SYNCPLAY	Explanation
0	Disenable to synchronization (Default)
1	Enable to synchronization

3.3.7 Relative Tempo register (RTEMPO)

The register is to set data to relatively change tempo of sound generator from original. Bit 7 indicate sign, "0" measn puls, "1" measn minus. Tempo is calculated by following formula.

"Actual tempo" = "Original tempo" * RTEMPO[6:0] * 5%

	7	6	5	4	3	2	1	0
RTEMPO	RTEMPO							
default	0	0	0	0	0	0	0	0

address: 0x010E
access: R/W

3.3.8 Transpose Setting register (TPOSE)

The register is to set transpose.

	7	6	5	4	3	2	1	0
TPOSE				TPOSE				
default	0	0	0	0	0	0	0	0

address: 0x0110
access: R/W

3.3.9 Current Time Setting register (CTCNT)

The register is to control current time.

	7	6	5	4	3	2	1	0
CTCNT	-	-	-	-	-	-	CTLOAD	CTMODE
default	-	-	-	-	-	-	0	0

address: 0x0112
access: R/W
[explanation of bit]

- **CTMODE**

CTMODE	Explanation
0	Output playback time (Default)
1	Output playback time in current position

The register is to decide output format of current position by sound generator. The LSI has two modes for output format.

When the bit is “0”, LSI output playback time. For example, relative tempo value is ignored to calculate time in the mode. Then, LSI output actual playback time.

On the other hand, when the bit is “1”, LSI output current time at current position. For example, relative tempo value is applied to calculate time in the mode. Then, LSI output playback position.

- **CTLOAD**

The bit is to stop updating CurrentTime register temporary. Before CurrentTime register is read,. The bit shall be set as “1”. And after CurrentTime register is read, please reset the bit to “0”.

3.3.10 Current Time register (CTIME3,2,1,0)

The register is to output current time of sound generator. Length of the register is 32 bit. Each byte is assigned like follow.

CTIME3: CTIME[31:24]
CTIME2: CTIME[23:16]
CTIME1: CTIME[15:8]
CTIME0: CTIME[7:0]

Notice:
Maximum of current time by the register is 12 hours. When LSI play longer music file than 12 hours, current time is reset to “0”. But playback is continuous.
When the register is read, please set CTLOAD bit of CTCNT register to “0”. After read, please set it to “1”.

	7	6	5	4	3	2	1	0
CTIME0	CTIME0							
default	0	0	0	0	0	0	0	0

address: 0x0114
access: R

	7	6	5	4	3	2	1	0
CTIME1	CTIME1							

	7	6	5	4	3	2	1	0
Default	0	0	0	0	0	0	0	0

address: 0x0116
access: R

	7	6	5	4	3	2	1	0
CTIME2	CTIME2							
Default	0	0	0	0	0	0	0	0

address: 0x0118
access: R

	7	6	5	4	3	2	1	0
CTIME3	CTIME3							
Default	0	0	0	0	0	0	0	0

address: 0x011A
access: R

3.3.11 LED Synchronization register (LEDE0, LED1, LED2, LED3)

The register is to output brightness of LED, when MIDI file include brightness data for LED. Format for LED is compatible with other sound generator by OKI. When any value is changed, LSI output interrupt request.

	7	6	5	4	3	2	1	0
LED0	LED0							
Default	0	0	0	0	0	0	0	0

address: 0x011C
access: R

	7	6	5	4	3	2	1	0
LED1	LED1							
Default	0	0	0	0	0	0	0	0

address: 0x011E
access: R

	7	6	5	4	3	2	1	0
LED2	LED2							
default	0	0	0	0	0	0	0	0

address: 0x0120
access: R

	7	6	5	4	3	2	1	0
LED3	LED3							
default	0	0	0	0	0	0	0	0

address: 0x0122
access: R

3.3.12 VIB Synchronization register (VIB)

The register is to output strength of vibrator, when MIDI file include strength of vibrator. Format for vibrator is compatible with other sound generator by OKI. When any value is changed, interrupt request takes place.

	7	6	5	4	3	2	1	0
VIB	VIB							

default	0	0	0	0	0	0	0	0

address: 0x0124
access: R

3.3.13 Sync Count register (SYNCC)

The register is to output counted number by SYNC signal in MIDI file. When the register is changed, LSI output interrupt request.

	7	6	5	4	3	2	1	0
SYNCC	SYNCC							
default	0	0	0	0	0	0	0	0

address: 0x0126
access: R

3.3.14 Sound Generator Sync Status register (SGSYNCST)

The register is to output synchronization status by sound generator. When LED0, LED1, LED3, VIB and SYNC registers are changed, each bit is set to “1”. When “1” is written to bit, the bit is reset to “0”.

	7	6	5	4	3	2	1	0
SGSYNC	-	-	SYNC	VIB	LED3	LED2	LED1	LED0
default	-	-	0	0	0	0	0	0

address: 0x0128
access: R/W

3.4 MP3 register

3.4.1 MP3 FIFO register (MP3FIFO)

The register is FIFO memory to input MP3 data. Before playback of MP3, please clear MP3 FIFO by MP3FIFOCLR.

	7	6	5	4	3	2	1	0
MP3FIFO	MP3FIFO							
default	-	-	-	-	-	-	-	-

address: 0x0200
access: W

3.4.2 MP3 FIFO Threshold register (MP3FIFOT0, MP3FIFOT1)

The register is to set threshold of MP3 FIFO memory. MP3 FIFO threshold register has 11bit. Each bit is assigned as below.
MP3FIFOT1 : MP3FIFOT[10:8]
MP3FIFOT0 : MP3FIFOT[7:0]

	7	6	5	4	3	2	1	0
MP3FIFOT1	-	-	-	-	-	MP3FIFOT1		
default	-	-	-	-	-	0	0	0

address: 0x0204
access: R/W

	7	6	5	4	3	2	1	0
MP3FIFOT0	MP3FIFOT0							
default	0	0	0	0	0	0	0	0

address: 0x0202
access: R/W

3.4.3 MP3 FIFO Clear register (MP3FIFOCLR)

The register is to clear MP3 FIFO. When write “1” to the bit, the both of MP3 FIFO and MP3 decoder is reset. Please clear MP3 FIFO before and after playback of MP3.

	7	6	5	4	3	2	1	0
MP3FIFOCLR	-	-	-	-	-	-	-	MP3FIFOCLR
default	-	-	-	-	-	-	-	-

address: 0x0206
access: W

3.4.4 MP3FIFO Status register (MP3FIFOST)

The register is output status of MP3 FIFO.

	7	6	5	4	3	2	1	0
MP3FIFOST	-	-	-	-	-	MP3FFULL	MP3FTHR	MP3FEMPTY
default	-	-	-	-	-	0	1	1

address: 0x0208
access: R
[Explanation of bit]

- **MP3FEMPTY**

When the bit is “1”, MP3 FIFO is empty. When the bit is “0”, MP3 FIFO is not empty.

- **MP3FTHR**

When the bit is “1”, number of remains in MP3 FIFO is less than threshold of MP3 FIFO.

- **MP3FFULL**

When the bit is “1”, MP3 FIFO is full. When it is “0”, MP3 FIFO is not full.

3.4.5 MP3 Control register (MP3CNT)

The register is to control MP3.

	7	6	5	4	3	2	1	0
MP3CNT	-	-	-	-	-	-	MP3OUT	MP3START
default	-	-	-	-	-	-	0	0

address: 0x020A
access: R/W

[Explanation of bit]

- **MP3START**

The bit is to start or stop MP3 decoding. When the bit is “1”, MP3 file in MP3 FIFO is decoded. Before the bit is set to “1”, MP3 FIFO shall be full.

MP3START	Explanation
0	Stop MP3 decoding (Default)
1	Start MP3 decoding

- **MP3OUT**

The bit is to control PCM output from MP3. When the bit is “0”, MP3 decoder does not output PCM. When the bit is “1”, MP3 decoder output PCM. Please set “1” to the bit under following conditions.

- MP3FRMST bit is “1”.
- MP3EMPTY bit is “0”.
- MP3OBUF bit is “1”.

When MP3 playback is in pause, please set the bit to “0”.

MP3OUT	Explanation
0	disenable to output PCM from MP3 (Default)
1	enable to output PCM from MP3

3.4.6 MP3 Dual Channel Select register (MP3CHSEL)

The register is to control MP3. Please see following table for detail.

	7	6	5	4	3	2	1	0
MP3CNT	-	-	-	-	-	-	MP3CHSEL	
default	-	-	-	-	-	-	0	0

address: 0x020C
access: R/W

MP3CHSEL	Explanation
0	Output the both of Left and right. (Default)
1	Output main(left) from left and right.
2	Output sub(right) from left and right.
3	forbid to set

3.4.7 MP3 FIFO Requested Number register (MP3FIFON1)

The registers are to output requested number of MP3 FIFO.
They consist of 11bit. MP3FIFON1 register is assigned upper 8bit.
MP3FIFON1 : MP3FIFON[10:3]
When interrupt request from MP3 FIFO occurs, please enter MP3 data to MP3 FIFO that number is written in this register.

	7	6	5	4	3	2	1	0
MP3FIFON1	MP3FIFON1							
default	0	0	0	0	0	0	0	0

address: 0x0210
access: R

Notice:
The register output “0”, when MP3 FIFO is the both of empty and full.

3.4.8 MP3 Error register (MP3ERR)

	7	6	5	4	3	2	1	0
MP3ERR	-	-	-	-	-	MP3ISR	MP3ILR	MP3IBR
default	-	-	-	-	-	0	0	0

address: 0x0212
access: R/W
[explanation of bit]

- **MP3IBR**

When LSI detects MP3 bit rate that the LSI does not support, the bit is set to “1”. When the bit becomes “1”, LSI output interrupt request. Please stop playback and initialize MP3 decoder in this case. In order to clear, please write "1" to the bit.

MP3IBR	Explanation
0	Does not detect bit rate LSI does not support (Default)
1	Detect bit rate LSI does not support

- **MP3ILR**

When LSI detects MP3 layer that the LSI does not support, the bit is set to “1”. When the bit becomes “1”, LSI output interrupt request. Please stop playback and initialize MP3 decoder in this case. In order to clear, please write "1" to the bit.

MP3ILR	Explanation
0	Does not detect layer LSI does not support (Default)
1	Detect layer LSI does not support

- **MP3ISR**

When LSI detects sampling rate that the LSI does not support, the bit is set to “1”. When the bit becomes “1”, LSI output interrupt request. Please stop playback and initialize MP3 decoder in this case. In order to clear, please write "1" to the bit.

MP3ISR	Explanation
0	Does not detect sampling rate LSI does not support(Default)
1	Detect sampling rate LSI does not support

3.4.9 MP3 Status register (MP3STAT)

The register is to output status of MP3 decoder.

	7	6	5	4	3	2	1	0
MP3STAT	-	-	-	-	-	-	MP3OBUF	Reserved
default	-	-	-	-	-	-	0	1

address: 0x0216
access: R/W

[Explanation of bit]

- **Reserved**

- **MP3OBUF**

Please see below for detail. In order to clear, please write "1" to the bit.

MP3OBUF	Explanation
0	output buffer is not full. (Default)
1	output buffer is full.

3.4.10 MP3 Interrupt Mode register (MP3DRQSEL)

The register is to decide way of MP3 data request.

	7	6	5	4	3	2	1	0
MP3DRQSEL	-	-	-	-	-	-	-	MP3DRQSEL
default	-	-	-	-	-	-	-	0

address: 0x0218
access: R/W

[Explanation of bit]

- **MP3DRQSEL**

MP3DRQSEL	Explanation
0	DREQ & FIFO Empty (Default)
1	FIFO threshold

3.5 ADPCM register

3.5.1 ADPCM FIFO register (ADFIFO)

The register is ADPCM FIFO to write ADPCM data.

	7	6	5	4	3	2	1	0
ADFIFO	ADFIFO							
default	-	-	-	-	-	-	-	-

address: 0x0300
access: W

3.5.2 ADPCM FIFO Threshold register (ADFIFOT0, ADFIFOT1)

The register is to set threshold of ADPCM FIFO memory. ADPCM FIFO threshold register has 11bit. Each bit is assigned as below.
ADFIFOT1 : ADFIFOT[10:8]
ADFIFOT0 : ADFIFOT[7:0]

	7	6	5	4	3	2	1	0
ADFIFOT1	-	-	-	-	-	ADFIFOT1		
default	-	-	-	-	-	0	0	0

address: 0x0304
access: R/W

	7	6	5	4	3	2	1	0
ADFIFOT0	ADFIFOT0							
default	0	0	0	0	0	0	0	0

address: 0x0302
access: R/W

3.5.3 ADPCM FIFO Clear register (ADFIFOCLR)

The register is to clear ADPCM FIFO. When write “1” to the bit, the both of ADPCM FIFO and ADPCM decoder shall be reset. Please clear ADPCM FIFO before playback of ADPCM.

	7	6	5	4	3	2	1	0
ADFIFOCLR								ADFIFOCLR
default	-	-	-	-	-	-	-	-

address: 0x0306
access: W

3.5.4 ADPCM FIFO Status register (ADFIFOST)

The register is output status of ADPCM FIFO.

	7	6	5	4	3	2	1	0
ADFIFOST	-	-	-	-	-	ADFFULL	ADFTHR	ADFEMPTY
default	-	-	-	-	-	0	1	1

address: 0x0308
access: R
[Explanation of bit]

- **ADFEMPTY**

When the bit is “1”, ADPCM FIFO is empty. When the bit is “0”, ADPCM FIFO is not empty.

- **ADFTHR**

When the bit is “1”, number of remains in ADPCM FIFO is less than threshold of ADPCM FIFO.

- **ADFFULL**

When the bit is “1”, ADPCM FIFO is full. When it is “0”, ADPCM FIFO is not full.

3.5.5 ADPCM Control register0 (ADPCNT0)

The register is to control ADPCM.

	7	6	5	4	3	2	1	0
ADPCNT0	-	-	-	-	-	-	ADPPAUSE	ADPSTART
default	-	-	-	-	-	-	0	0

address: 0x030A
access: R/W

[Explanation of bit]

- **ADPSTART**

The bit is to start or stop ADPCM playback. Before the bit is set to “1”, ADPCM FIFO shall be full.

ADPSTART	Explanation
0	Stop ADPCM playback (Default)
1	Start ADPCM playback

- **ADPPAUSE**

The bit is to set or release pause of ADPCM.

ADPSTART	Explanation
0	release pause of ADPCM (Default)
1	set pause of ADPCM.

3.5.6 1ADPCM control register1 (ADPCNT1)

The register is to set sampling frequency and data format.

	7	6	5	4	3	2	1	0
ADPCNT1	-	APFM		ADPMODE			ADPFRQ	
default	-	0	0	0	0	0	0	0

address: 0x030C
access: R/W

[Explanation of bit]

- **ADPFRQ**

The bits are to set sampling frequency. The bits must be set to “0”, except ADPCM playback. Because SRC block use this register.

ADPFRQ	explanation
0	4.0kHz (Default)
1	5.333kHz
2	6.4kHz
3	8.0kHz
4	10.666kHz
5	12.8kHz
6	16.0kHz
7	32.0kHz

- **ADPMODE**

The register is to set format.

ADPMODE	explanation
0	4-bit ADPCM (Default)

1	2-bit ADPCM
2	16-bit PCM
3	8-bit PCM

- **APFM**

The register is to set PCM format in detail.

APFM	explanation
0	2's complement When 16bit PCM is played, upper byte is sent at first and lower byte is sent secondly. (Default)
1	2's complement When 16bit PCM is played, lower byte is sent at first and upper byte is sent secondly.
2	Straight Binary When 16bit PCM is played, upper byte is sent at first and lower byte is sent secondly.
3	Straight Binary When 16bit PCM is played, lower byte is sent at first and upper byte is sent secondly.

3.6 SAI register

3.6.1 SAI Control register 0 (SAICON0)

The register is to set format to receive or transmit audio data though SAI. Please the register shall not be changed, when SAI actives.

	7	6	5	4	3	2	1	0
SAICON0	-	MSBI	ISSCKI	AFOI		DLYI	WSLI	RUN
default	-	0	0	0	0	0	0	0

address: 0x0400
access: R/W

[Explanation of bit]

- **RUN**

The bit is to control start or stop.

RUN	Explanation
0	stop receiving or transmitting(Default)
1	start receiving or transmitting

- **WSLI**

The bit is to decide level to receive or transmit left channel of audio data.

WSLI	Explanation
0	Left channel of audio data is received or transmitted, while LRCLK is low level. (Default)
1	Left channel of audio data is received or transmitted, While LRCLK is high level.

- **DLYI**

The bit is to set serial audio data with or without 1 bit delay.

DLYI	Explanation
0	with 1bit delay (Default)
1	without 1bit delay

- **AFOI**

The bits are to decide left justified mode or right justified mode.

- **ISSCKI**

The bit is to decide number of BCLK clock in one sampling frequency.

AFOI	ISSCKI	Explanation
00	0	BCLK 32 clocks (Default)
01		BCLK 32 clocks
10		BCLK 32 clocks
11		BCLK 32 clocks
00	1	BCLK 32 clocks
01		BCLK 64 clocks left justified
10		BCLK 64 clocks right justified
11		BCLK 32 clocks

- **MSBI**

The bit is to decide MSB first or LSB first for serial audio data.

MSBI	Explanation
0	MSB first (Default)
1	LSB first

3.6.2 SAI Control register1(SAICON1)

The register is to control SAI block. The register must be set to "0", when SAI block is used. Please the register shall not be changed, when SAI actives.

	7	6	5	4	3	2	1	0
SAICON1	-	-	-	-	-	-	-	MST
default	-	-	-	-	-	-	-	1

address: 0x0402
access: R/W

3.6.3 SAI Sampling Frequency register(SAIFRQ)

The register is to set sampling frequency of which SAI receives or transmits audio data. The register must be set before receiving audio data from SAI. When SAI is not use, the register must be set as "0". Please the register shall not be changed, when SAI actives.

	7	6	5	4	3	2	1	0
SAICON1	-	-	-	-	SAIFRQ			
default	-	-	-	-	0	0	0	0

address: 0x0404
access: R/W

SAIFRQ	Explanation
0x0	8kHz (Default)
0x1	11.025kHz
0x2	12kHz
0x3	16kHz
0x4	22.05kHz
0x5	24kHz
0x6	32kHz
0x7	44.1kHz
0x8	48kHz
0x9-0xF	Forbid to set

3.6.4 SAI Control register2 (SAICON2)

The register is to control SAI transmitter.

	7	6	5	4	3	2	1	0
SAICON2	—	—	—	—	Reserved	Reserved	Reserved	SAIOUT
default	—	—	—	—	0	0	0	0

address: 0x0406
access: R/W

[Explanation of bit]

- **SAIOUT**

This bit is to select transmitter enable or not. When start transmit, set "1" to RUN bit of SAICON0.

SAIOUT	Explanation
0	Transmitter disenable (Default)
1	Transmitter enable

- **Reserved**

These bits shall be set to “0”.

3.7 SRC register

3.7.1 Playback Select register (MIXSEL)

The register is to decide either of ADPCM, MP3 or SAI with sound generator.

	7	6	5	4	3	2	1	0
MIXSEL	-	-	-	-	SAI BYPASS	MP3 BYPASS	MIXSEL	
default	-	-	-	-	0	0	0	0

address: 0x0500
access: R/W

[Explanation of bit]

- **MIXSEL**

The bits are to decide sound source mixed with sound generator. In the case of single playback of MP3 or SAI by MP3BYPASS bit or SAIBYPASS bit, the bits are ignored.

MIXSEL	explanation
0	single playback of sound generator(Default)
1	ADPCM is mixed with sound generator.
2	MP3 is mixed with sound generator.
3	SAI is mixed with sound generator. In the event, SAI sampling frequency is fixed as 44.1kHz.

- **MP3BYPASS**

The bit is to decide whether audio data from MP3 bypasses MIX and SRC block, or not. When the bit is “1”, SAIBYPASS bit and MIXSEL bit are ignored. Please the bit shall not be changed during playback.

The bit is used for reducing power consumption of MP3 playback. Bypassing mode shall be lower than mixing mode.

MP3BYPASS	Explanation
0	Mixing mode. SRC and MIX block is used.(Default)
1	Bypass mode. MP3 data bypasses SRC and MIX blocks..

- **SAIBYPASS**

The bit is to decide whether audio data though SAI bypasses MIX and SRC block, or not. When the bit is “1”, MIXSEL bit are ignored and MP3BYPASS bit must be “0”. Please the bit shall not be changed during playback.

The bit is used for reducing power consumption of SAI playback. Bypassing mode shall be lower than mixing mode.

SAIBYPASS	Explanation
0	Mixing mode. SRC and MIX block is used.(Default)
1	Bypasses mode for SAI. Data though SAI bypasses SRC and MIX blocks.

3.7.2 SG Volume register (SGVOL)

The register is to set volume of sound generator. The volume is used to balance between sound generator and other audio source.

	7	6	5	4	3	2	1	0
SGVOL	-	-	-	SGVOL				
default	-	-	-	0	0	0	0	0

address: 0x0502
access: R/W

SGVOL	Level (dB)	SGVOL	Level (dB)
0x00	0 (Default)	0x0E	-28
0x01	-2	0x0F	-30
0x02	-4	0x10	-32
0x03	-6	0x11	-34
0x04	-8	0x12	-36
0x05	-10	0x13	-38
0x06	-12	0x14	-40
0x07	-14	0x15	-42
0x08	-16	0x16	-44
0x09	-18	0x17	-46
0x0A	-20	0x18	-48
0x0B	-22	0x19	Mute
0x0C	-24	:	Mute
0x0D	-26	0x1F	Mute

Notice:
Output volume is changed soon after register is changed. Therefore, volume is changed largely suddenly, pop noise may arise.

3.7.3 SG Balance register (SGBAL)

The register is to balance between left and right of sound generator.

	7	6	5	4	3	2	1	0
SGBAL	SGBALL				SGBALR			
default	0	0	0	0	0	0	0	0

address: 0x0504
access: R/W

[Explanation of bit]

- **SGBALL**

The bits are to change left volume of sound generator. Please see following table for detail.

SGBALL	Level (dB)	SGBALL	Level (dB)
0x00	0 (Default)	0x08	-16
0x01	-2	0x09	-18
0x02	-4	0x0A	-20
0x03	-6	0x0B	-22
0x04	-8	0x0C	-24
0x05	-10	0x0D	-26
0x06	-12	0x0E	-28
0x07	-14	0x0F	Mute

- **SGBALR**

The bits are to change right volume of sound generator. Since the volume is same as SGBALL bits, please see the table above.

Notice:
Output volume is changed soon after the register is changed. Therefore, volume is changed largely suddenly, pop noise may arise.

3.7.4 SRC Volume register (SRCVOL)

The register is to set volume though SRC block. It is used to balance volume with sound generator.

7	6	5	4	3	2	1	0

SRCVOL	-	-	-	SRCVOL				
default	-	-	-	0	0	0	0	0

address: 0x0506
access: R/W

SRCVOL	Level (dB)	SRCVOL	Level (dB)
0x00	0 (Default)	0x0E	-28
0x01	-2	0x0F	-30
0x02	-4	0x10	-32
0x03	-6	0x11	-34
0x04	-8	0x12	-36
0x05	-10	0x13	-38
0x06	-12	0x14	-40
0x07	-14	0x15	-42
0x08	-16	0x16	-44
0x09	-18	0x17	-46
0x0A	-20	0x18	-48
0x0B	-22	0x19	Mute
0x0C	-24	:	Mute
0x0D	-26	0x1F	Mute

Notice:
Output volume is changed soon after the register is changed. Therefore, volume is changed largely suddenly, pop noise may arise.

3.7.5 SRC Balance register (SRCBAL)

The register is to balance between left and right though SRC.

	7	6	5	4	3	2	1	0
SRCPAN	SRCBALL				SRCBALR			
default	0	0	0	0	0	0	0	0

address: 0x0508
access: R/W

[Explanation of bit]

- **SRCBALL**

The bits are to change left volume though SRC. Please see following table for detail.

SRCBALL	Level (dB)	SRCBALL	Level (dB)
0x00	0 (Default)	0x08	-16
0x01	-2	0x09	-18
0x02	-4	0x0A	-20
0x03	-6	0x0B	-22
0x04	-8	0x0C	-24
0x05	-10	0x0D	-26
0x06	-12	0x0E	-28
0x07	-14	0x0F	Mute

- **SRCBALR**

The bits are to change right volume though SRC. Since the volume is same as SRCBALL bits, please see the table above.

Notice:
Output volume is changed soon after the register is changed. Therefore, volume is changed largely suddenly, pop noise may arise.

3.7.6 POP Noise Filter Control register (POPCNT)

The register is to enable or disenable pop noise filter. Pop noise is reduced in this mode, when playback is started, stopped or paused. Because audio level shifts to signal ground gently.

	7	6	5	4	3	2	1	0
POPCNT	-	-	-	-	-	-	-	SRCPOP
default	-	-	-	-	-	-	-	0

address: 0x050A
access: R/W

SRCPOP	Explanation
0	Pop noise filter enables. (Default)
1	Pop noise filter disenables.

3.8 3D surround register

3.8.1 SRS3D Enable register (SRS3DEN)

The register is to enable or disenable SRS3D. When the bit is set to “1”, SRS3D is enabled. When “0”, SRS3D is disenabled.

	7	6	5	4	3	2	1	0
SRS3DEN	-	-	-	-	-	-	-	SRS3DEN
default	-	-	-	-	-	-	-	0

Address: 0x0600
Access: R/W

SRS3DEN	Explanation
0	Disenable SRS3D(Default)
1	Enable SRS3D

Notice:
SRS3D support over 16kHz as sampling frequency. Then, if SRS3D is applied to below 16kHz, effect is less expectative.

3.8.2 SRS3D Mode register(SRS3DMODE)

The register is to set mode of SRS3D.

	7	6	5	4	3	2	1	0
SRS3DMODE	-	-	-	-	-	-	-	SRS3DMODE
default	-	-	-	-	-	-	-	0

Address: 0x0602
Access: R/W

SRS3DMODE	Explanation
0	This mode supports SRS3D headphone.
1	This mode supports SRS3D extreme mode.

Notice:
When the register is changed, it is recommended that SRS3D is disenabled. Because, it is possible to include pop noise.

3.8.3 SRS3D Control register (SRS3DSWCNT)

This register is to set strength of SRS3D headphone.

	7	6	5	4	3	2	1	0
SRS3DSWCNT	-	SRS3DSWCNT						
default	-	1	1	0	0	1	1	0

Address: 0x0604
Access: R/W

3.8.4 SRS3D Extreme Control register (SRS3DEWCNT)

This register is to set strength of SRS3D Extreme which is optimized to stereo speaker.

	7	6	5	4	3	2	1	0
SRS3DEWCNT	-	SRS3DEWCNT						
default	-	1	1	0	0	1	1	0

Address: 0x0606
Access: R/W

3.9 Equalizer register

3.9.1 EQ Enable register(EQEN)

The register is to enable or disenable equalizer.

	7	6	5	4	3	2	1	0
EQEN	-	-	-	-	-	-	-	EQEN
default	-	-	-	-	-	-	-	0

Address: 0x0700
Access: R/W

EQEN	Explanation
0	Disenable equalizer(Default)
1	Enable equalizer

Notice: EQ support over 16kHz as sampling frequency. Then, if EQ is applied to below 16kHz, effect is less expectative.

3.9.2 EQ Band 0 Gain register(EQGAIN0)

The register is to set gain for band 0 of equalizer

	7	6	5	4	3	2	1	0
EQGAIN0	-	-	-	EQGAIN0				
default	-	-	-	0	1	0	1	0

Address: 0x0702
Access: R/W

Please see following table for detailed gain.

EQGAIN0	Gain	EQGAIN0	Gain
0x00	+10dB	0x0B	-1dB
0x01	+9dB	0x0C	-2dB
0x02	+8dB	0x0D	-3dB
0x03	+7dB	0x0E	-4dB
0x04	+6dB	0x0F	-5dB
0x05	+5dB	0x10	-6dB
0x06	+4dB	0x11	-7dB
0x07	+3dB	0x12	-8dB
0x08	+2dB	0x13	-9dB
0x09	+1dB	0x14	-10dB
0x0A	0dB		

3.9.3 EQ Band 1 Gain register(EQGAIN1)

The register is to set gain for band 1 of equalizer. As for gain, please see table in EQ Band 0.

	7	6	5	4	3	2	1	0
EQGAIN1	-	-	-	EQGAIN1				
default	-	-	-	0	1	0	1	0

Address: 0x0704
Access: R/W

3.9.4 EQ Band 2 Gain register(EQGAIN2)

The register is to set gain for band 2 of equalizer. As for gain, please see table in EQ Band 0.

	7	6	5	4	3	2	1	0
EQGAIN2	-	-	-	EQGAIN2				

default	-	-	-	0	1	0	1	0

Address: 0x0706
Access: R/W

3.9.5 EQ Band 3 Gain register(EQGAIN3)

The register is to set gain for band 3 of equalizer. As for gain, please see table in EQ Band 0.

	7	6	5	4	3	2	1	0
EQGAIN3	-	-	-	EQGAIN3				
default	-	-	-	0	1	0	1	0

Address: 0x0708
Access: R/W

3.9.6 EQ Band 4 Gain register(EQGAIN4)

The register is to set gain for band 4 of equalizer. As for gain, please see table in EQ Band 0.

	7	6	5	4	3	2	1	0
EQGAIN4	-	-	-	EQGAIN4				
default	-	-	-	0	1	0	1	0

Address: 0x070A
Access: R/W

Following table shows the relation between band number and frequency.

Sampling frequency (kHz)	band0		band1		band2		band3		band4		
	cross	center	cross	center	cross	center	cross	center	cross	center	cross
16000	30	-	150	281	527	987	1850	3467	6498	-	7999
22050	30	-	197	369	691	1295	2428	4550	8528	-	11024
24000	30	-	234	439	823	1542	2890	5417	10152	-	11999
32000	30	-	200	400	800	1600	3200	6400	12800	-	15999
44100	30	-	250	500	1000	2000	4000	8000	16000	-	22049
48000	30	-	250	500	1000	2000	4000	8000	16000	-	23999

center means the center frequency of each band.

3.10 DAC and Headphone amplifier register

3.10.1 Output Control register (OUTCNT)

The register is to control headphone amplifier and audio output amplifier.

	7	6	5	4	3	2	1	0
DACCNT	-	-	-	-	-	PDDAC	PDHP	PDANA
default	-	-	-	-	-	0	0	0

Address: 0x0800
Access: R/W

[Explanation of bit]

- **PDANA**

The bit is to enable or disenable audio output amplifier.

PDANA	Explanation
0	Disenable Audio Output amplifier (Default)
1	Enable Audio Output amplifier

- **PDHP**

The bit is to enable or disenable headphone amplifier.

PDHP	Explanation
0	Disenable headphone amplifier (Default)
1	Enable headphone amplifier

- **PDDAC**

The bit is to enable or disenable Audio DAC.

PDDAC	Explanation
0	Disenable Audio DAC(Default)
1	Enable Audio DAC

3.10.2 Headphone Setting register (HPMOD)

The register is to control detail of headphone amplifier. Please set the register, while audio DAC and headphone amplifier is in power down.

	7	6	5	4	3	2	1	0
HPMOD	-	-	-	-	PDDRVSPD		Reserved	COMON
default	-	-	-	-	0	1	0	0

Address: 0x0802
Access: R/W

[Explanation of bit]

- **COMON**

The bit is to decide whether COM pin of headphone amplifier is enabled or not.

COMON	Explanation
0	COM pin is Hi-Z(Default)
1	COM pin output signal ground.

- **Reserved**

The bit shall be set to "0".

- **PDDRVSPD**

The bits are to set time between power down and power up for headphone amplifier in order to reduce pop noise of headphone. When duration is longer, noise shall be smaller.

PDDRVSPD	Explanation

0	23ms@44.1kHz, 22.05kHz, 11.025kHz 21ms@48kHz, 24kHz, 12kHz 32ms@32kHz, 16kHz, 8kHz
1	46ms@44.1kHz, 22.05kHz, 11.025kHz 42ms@48kHz, 24kHz, 12kHz 64ms@32kHz, 16kHz, 8kHz (Default)
2	92ms@44.1kHz, 22.05kHz, 11.025kHz 85ms@48kHz, 24kHz, 12kHz 128ms@32kHz, 16kHz, 8kHz
3	forbid

3.10.3 Audio Output Setting register (ANAMOD)

The bits are to set power up time for Audio output amplifier in order to reduce pop noise of audio output amplifier. Please set the register while audio output amplifier is in power down.

Unit of time is 10ms. Power up time can be calculated below.

Time = ANAMOD * 10ms

	7	6	5	4	3	2	1	0
ANAMOD	-	-	-	ANAMOD				
default	-	-	-	0	0	1	0	1

Address: 0x0804
Access: R/W

3.10.4 DAC Volume register (DACLVL)

The register is to set volume of DAC.

	7	6	5	4	3	2	1	0
DACLVL	-	DACLVL						
default	-	0	0	0	0	0	0	0

Address: 0x0806
Access: R/W

Please see following table for detail.

DACLVL	Level (dB)	DACLVL	Level (dB)
0x00	0 (Default)	:	:
0x01	-1	:	:
0x02	-2	0x48	-72
0x03	-3	0x49	Mute
0x04	-4	:	:
0x05	-5	:	:
0x06	-6	0x7E	Mute
0x07	-7	0x7F	Mute

3.10.5 DAC Balance register (DACBAL)

The register is to set volume balance for DAC. DACBALL is for left channel, and DACBALR is for right channel.

	7	6	5	4	3	2	1	0
DACBAL	DACBALL				DACBALR			

default	0	0	0	0	0	0	0	0

Address: 0x0808
Access: R/W

Please see following table for detail.

DACBALL DACBALR	Level (dB)	DACBALL DACBALR	Level (dB)
0x00	0 (Default)	0x08	-16
0x01	-2	0x09	-18
0x02	-4	0x0A	-20
0x03	-6	0x0B	-22
0x04	-8	0x0C	-24
0x05	-10	0x0D	-26
0x06	-12	0x0E	-28
0x07	-14	0x0F	Mute

3.10.6 DAC Mute register (DACMUTE)

The register is to set mute of DAC.

	7	6	5	4	3	2	1	0
DACMUTE	-	-	-	-	-	-	DACMUTE	
default	-	-	-	-	-	-	1	1

Address: 0x080A
Access: R/W

DACMUTE	Explanation
0	normal
1	Mute only left channel.
2	Mute only right channel.
3	Mute the both channel(Default)

3.10.7 DAC Volume Adjusting Time register (DACVOLST)

The register is to set unit time to change volume from original to target. The function applies to DACVLV, DACBAL and DACMUTE.

The register shall be changed while DAC and headphone amplifier is in power down.

	7	6	5	4	3	2	1	0
DACVOLST	-	-	-	-	-	-	DACVOLST	
default	-	-	-	-	-	-	0	1

Address: 0x080C
Access: R/W

DACVOLST	Explanation
0	1dB/ (128 / sampling frequencies)
1 (default)	1dB/ (32 / sampling frequencies)
2	1dB/ (8 / sampling frequencies)
3	1dB/ (1 / sampling frequencies)

3.10.8 Output Status register (OUTSTAT)

The register is to output status of audio output amplifier, headphone amplifier, and DAC.

	7	6	5	4	3	2	1	0
DACSTAT	-	-	-	-	-	DACBSY	HPBSY	ANABSY
default	-	-	-	-	-	0	0	0

Address: 0x080E
Access: R/W

[Explanation of bit]

- **ANABSY**

The bit is set to “1”, when status of audio output amplifier stables to the active. When the bit becomes “1”, ORDYST bit for interrupt request is set. The bit can be cleared, when write “1” to the bit.

- **HPBSY**

The bit is set to “1”, when status of headphone amplifier stables to power down or the active. When the bit becomes “1”, ORDYST bit for interrupt request is set. The bit can be cleared, when write “1” to the bit.

- **DACBSY**

The bit is set to “1”, when volume is reached to target. When the bit becomes “1”, ORDYST bit for interrupt request is set. The bit can be cleared, when write “1” to the bit.

Notice:
When volume is not changed, the bit is not set. For example, when mute register is set during mute by volume register, the bit is not set.

3.11 Interrupt register

3.11.1 Interrupt Module register (IRQMOD)

The register is to determine which block output interrupt request.

	7	6	5	4	3	2	1	0
IRQMOD	-	-	-	SGIRQ	MP3IRQ	ADPIRQ	SAIIRQ	ANAIRQ
default	-	-	-	1	1	1	0	0

Address: 0x0900
Access: R
[Explanation of bit]

- **ANAIRQ**

The bit is set to "1", when analog interrupt status register changed. In order to clear this bit, analog interrupt register (ANAIRQST) and/or output status register (OUTSTAT) shall be clear.

- **SAIIRQ**

The bit is set to "1", when interrupt request of SAI block occurs. In order to clear this bit, please clear SAI interrupt register.

- **ADPIRQ**

The bit is set to "1", when interrupt request of ADPCM block occurs. In order to clear this bit, please clear ADPCM interrupt register.

- **MP3IRQ**

The bit is set to "1", when interrupt request of MP3 occurs. In order to clear this bit, please clear MP3 interrupt register.

- **SGIRQ**

The bit is set to "1", when interrupt request from sound generator occurs. In order to clear this bit, please clear SG Interrupt register.

3.11.2 Analog Interrupt register(ANAIRQST)

The register is to determine interrupt related to analog block.

	7	6	5	4	3	2	1	0
ANAIRQST	-	-	-	-	ORDYST	Reserved	APLLLOCKST	LPLLLOCKST
default	-	-	-	-	0	0	0	0

Address: 0x0902
Access: R/W

[Explanation of bit]

- **LPLLLOCKST**

When logic PLL is stable, the bit is set to "1". In order to clear, please write "1" to the bit.

- **APLLLOCKST**

When Audio PLL is stable, the bit is set to "1". In order to clear, please write "1" to the bit.

- **Reserved**

- **ORDYST**

When any bit in output status register (OUTSTAT) is "1", the bit is "1". In this case, either of headphone amplifier, audio output amplifier or DAC can accept next operation. In order to clear this bit, please clear output status register (OUTSTAT).

3.11.3 SAI Interrupt register(SAIIRQST)

The register is to check interrupt status of SAI. When SAI playback finishes, the bit is set to "1". When clear the bit, please write "1" to the bit.

	7	6	5	4	3	2	1	0
SAIIRQST	-	-	-	-	-	-	-	SAIMONST
default	-	-	-	-	-	-	-	0

Address: 0x0904
Access: R/W

3.11.4 ADPCM Interrupt register(ADPIRQST)

The register is to determine interrupt of ADPCM.

	7	6	5	4	3	2	1	0
MP3IRQST	-	-	-	-	-	-	ADPFIFOST	ADPMONST
default	-	-	-	-	-	-	1	0

Address: 0x0906
Access: R/W

[Explanation of bit]

- **ADPMONST**

When ADPCM playback finishes, the bit is set to "1". In order to clear the bit, please write "1" to the bit.

- **ADPFIFOST**

The bit is to show status of FIFO. Please see following table for detail. In order to clear the bit, please write "1" to the bit.

ADPFIFOST	Explanation
0	Remaining number of bytes in ADPCM FIFO is more than threshold of ADPCM FIFO (Default)
1	Remaining number of bytes in ADPCM FIFO is threshold of ADPCM FIFO and below.

3.11.5 MP3 Interrupt register(MP3IRQST)

The register is to determine interrupt of MP3.

	7	6	5	4	3	2	1	0
MP3IRQST	-	-	MP3ENDST	MP3FRMST	Reserved	MP3ERRST	MP3FIFODRQST	MP3MONST
default	-	-	0	0	0	0	1	0

Address: 0x0908
Access: R/W

[Explanation of bit]

- **MP3MONST**

The bit is "1", when MP3 playback stop or pause. In order to clear the bit, please write "1" to the bit.

- **MP3FIFODRQST**

Please see following table for detail.

MP3FIFODRQ	Explanation
0	MP3 does not request next data
1	MP3 requests next data(Default)

- **MP3ERRST**

The bit is "1", when the LSI can not play MP3 to be sent. In order to clear the bit, please clear MP3 Error register.

MP3ERRST	Explanation
0	MP3 file is not error. (Default)
1	MP3 file is error.

- **MP3FRMST**

The bit is set to “1”, when MP3 decoder detects sync word in MP3 file. When the bit is set to “1”, enable of Audio PLL can be set to “1”. In order to clear the bit, please write “1” to the bit.

MP3FRMST	Explanation
0	Does not detect sync word (Default)
1	Detect sync word

- **MP3ENDST**

When decoded PCM data is empty and MP3 FIFO is empty, the bit is set to “1”. The condition shall be end of playback.

MP3ENDST	Explanation
0	Other condition than follow(Default)
1	There is no decoded PCM data and MP3 data in MP3 FIFO.

3.11.6 SG Interrupt register(SGIRQST)

The register is to determine status of sound generator.

	7	6	5	4	3	2	1	0
SGIRQST	-	-	-	-	SGSYNCST	SGERRST	SGFIFOST	SGMONST
default	-	-	-	-	0	0	1	0

Address: 0x090A
Access: R/W

[Explanation of bit]

- **SGMONST**

The bit is set to “1” at the end of playback of sound generator.

- **SGFIFOST**

SGFIFOST	Explanation
0	Remain number of byte in SG FIFO is more than threshold of SG FIFO.
1	Remain number of byte in SG FIFO is threshold of SG FIFO and below. (Default)

- **SGERRST**

The bit is set to “1”, when MIDI file include error. In the case, please stop playback of sound generator.
In order to clear, please write “1” to the bit.

- **SGSYNCST**

The bit is set to “1”, when SYNC, LED, VIB and SYNC register. In the case, please determine what register is changed by SGSYNCST register. In order to clear this bit, please clear SGSYNCST register.

3.11.7 Analog Interrupt Enable register(ANAIRQ)

The register is to set enable or disenable interrupt by Analog Interrupt register (ANAIRQST). When the bit is “1”, interrupt is enabled. When the bit is “0”, interrupt is disenabled.

7	6	5	4	3	2	1	0

ANAIRQ	-	-	-	-	ORDY	Reserved	APLLLOCK	LPLLLOCK
default	-	-	-	-	0	0	0	1

Address: 0x090C
Access: R/W

[Explanation of bit]

- **LPLLLOCK**

The bit is to enable or disenable interrupt by LPLLLOCKST bit of Analog interrupt register.

LPLLLOCK	Explanation
0	Disenable logic PLL interrupt.
1	Enable logic PLL interrupt(Default)

- **APLLLOCK**

APLLLOCK	Explanation
0	Disenable audio PLL interrupt(Default)
1	Enable audio PLL interrupt

- **Reserved**

The bit shall be set to "0".

- **ORDY**

ORDY	Explanation
0	Disenable interrupt by ORDYST bit.(Default)
1	Enable interrupt by ORDYST bit

3.11.8 SAI Interrupt Enable register(SAIIRQ)

The register is to set enable or disenable interrupt by SAI interrupt register (SAIIRQST). When the bit is "1", interrupt is enabled. When the bit is "0", interrupt is disenabled.

	7	6	5	4	3	2	1	0
SAIIRQST	-	-	-	-	-	-	-	SAIMON
default	-	-	-	-	-	-	-	0

Address: 0x090E
Access: R/W

[Explanation of bit]

- **SAIMON**

SAIMON	Explanation
0	Disenable interrupt at the end of playback by SAI(Default)
1	Enable interrupt at the end of playback by SAI

3.11.9 ADPCM Interrupt Enable register(ADPIRQ)

The register is to set enable or disenable interrupt by ADPCM interrupt register (ADPIRQST). When the bit is "1", interrupt is enabled. When the bit is "0", interrupt is disenabled.

	7	6	5	4	3	2	1	0
SAIIRQST	-	-	-	-	-	-	ADPFIFO	ADPMON
default	-	-	-	-	-	-	0	0

Address: 0x0910
Access: R/W

[Explanation of bit]

- **ADPMON**

ADPMON	Explanation
0	Disenable interrupt at the end of playback by ADPCM(Default)
1	Enable interrupt at the end of playback by ADPCM

- **ADPFIFO**

ADPFIFO	Explanation
0	Disenable interrupt for data request of ADPCM (Default)
1	Enable interrupt for data request of ADPCM

3.11.10 MP3 Interrupt Enable register(MP3IRQ)

The register is to set enable or disenable interrupt by MP3 interrupt register (MP3IRQST). When the bit is "1", interrupt is enabled. When the bit is "0", interrupt is disenabled.

	7	6	5	4	3	2	1	0
MP3IRQ	-	-	MP3END	MP3FRM	Reserved	MP3ERR	MP3FIFODRQ	MP3MON
default	-	-	0	0	0	0	0	0

Address: 0x0912
Access: R/W

[Explanation of bit]

- **MP3MON**

MP3MON	Explanation
0	Disenable interrupt at the end of playback by MP3(Default)
1	Enable interrupt at the end of playback by MP3

- **MP3FIFODRQ**

MP3FIFO	Explanation
0	Disenable interrupt for data request of MP3(Default)
1	Enable interrupt for data request of MP3

- **MP3ERR**

MP3ERR	Explanation
0	Disenable interrupt for error of MP3 (Default)
1	Enable interrupt for error of MP3

- **Reserved**

The bit shall be set to "0".

- **MP3FRM**

MP3ERR	Explanation
0	Disenable interrupt for sync word of MP3(Default)
1	Enable interrupt for sync word of MP3

- **MP3END**

MP3ERR	Explanation
0	Disenable Interrupt at the end of MP3 playback (Default)
1	Enable Interrupt at the end of MP3 playback

3.11.11 SG Interrupt Enable register(SGIRQ)

The register is to set enable or disenable interrupt for sound generator.

	7	6	5	4	3	2	1	0
SGIRQ	-	-	-	-	SGSYNC	SGERR	SGFIFO	SGMON
default	-	-	-	-	0	0	0	0

Address: 0x0914
Access: R/W

[Explanation of bit]

- **SGMON**

SGMON	Explanation
0	Disenable interrupt at the end of playback by sound generator.(Default)
1	Enable interrupt at the end of playback by sound generator.

- **SGFIFO**

SGFIFO	Explanation
0	Disenable interrupt for data request by sound generator.(Default)
1	Enable interrupt for data request by sound generator.

- **SGERR**

SGERR	Explanation
0	Disenable interrupt for data error of sound generator.(Default)
1	Enable interrupt for data error of sound generator.

- **SGSYNC**

SGSYNC	Explanation
0	Disenable interrupt to synchronize LED, VIB, and so on.(Default)
1	Enable interrupt to synchronize LED, VIB, and so on.

4 MIDI Implementation Chart

Function name		Recognized	Remark
Basic Channel	POWER ON	1-16	
Mode	Message	Mode 3 Omni OFF, Poly	
	Altered	This is not included into the function.	
Note Number		0-127	
	True Voice	0-127	
Velocity	Note ON	This is included into the function. 9nH v = 1-127	
	Note Off	9nH v = 0, 8nH v = *1	
After Touch	Key's	X	
	Ch's	O	
Pitch Bender		O	Default: 2(Full scale) Max: 12(1 octave)
Control Change	0	O	Bank
	1	O	Modulation
	6,38	O	Data entry ・pitch bend sensitivity (MSB) ・fine tune (MSB/LSB) ・coarse tune (MSB)
	7	O	Volume
	10	O	Pan
	11	O	Expression
	64	O	Hold 1 (Sustain)
	100,101	O	RPN LSB, MSB 0:pitch bend sensitivity 1:fine tune 2:coarse tune
	120	O	All sounds off
	121	O	Reset all control
	123	O	All notes off
Program Change		0-127	
System Exclusive		O	
System Common	Song Position	X	
	Song Select	X	
	Tune	X	
System Real Time	Clock	X	
	Commands	X	
Aux Message	Local ON/OFF	X	
	Active Sense	X	
	Reset	X	

Mode 1: Omni On, Poly　　Mode 2: Omni On, Mono　　O: Supported
Mode 4: Omni Off, Poly　　Mode 4: Omni Off, Mono　　X: Not supported

4.1 Exclusive Message

4.1.1 Supported Message List

	Command	Message	Function
	Master volume	f0, 7f, <device id>(□), 04, 01, vL, vM, f7	Master MIDI Volume. Only the upper bit parameter (vM) [0x00-0x7F] is available in this system.
	Master balance	f0, 7f, <device id>(□), 04, 02, vL, vM ,f7	Master MIDI balance. Only the upper bit parameter (vM) [0x00(Left)-0x7F(Right)] is available in this system.
	MIP message	f0, 7f, <device id>(□), 0b, 01, {cc vv}, {cc vv} ... {cc vv}, {cc vv}, f7	Setting priority of channels for SP-MIDI.
	GM system on	f0, 7e, <device id>(□), 09, 01, f7	For reset the parameters of sound generator. Ref. [MIDI Reset Specification].
#	**Transpose**	f0, 5d, 0e, 08, 10, kkl, kkh, f7	Transpose. -128 - +127semitone. “kkl, kkh” can be just 1 byte.
#	**Master volume**	(f0, 5d, 0e, 08, 11, vv, f7	Master MIDI Volume. This message is compatible with the all of Oki sound generator LSI. The effect is same as Universal system exclusive above. The latest message becomes valid.
#	**Synchronous mode set**	(f0, 5d, 0e, 08, 12, md, d0, d1, f7	For setting sync between music playback and port operation.
#	**Touch correct**	f0, 5d, 0e, 08, 13, tt, f7	To add “tt” on the original velocity value in all note on message.
#	**ADPCM Sync-Play CUE**	f0, 5d, 0e, 08, 17, acue, f7	Output start playback cue to ADPCM decoder
#	**Effective Sounds**	f0, 5d, 0e, 08, 18, ch, tl, th, f7	To select sound effect or Chinese Instrument on assigned channel. It effects same as “Bank Select + Program Change”.
#	**Relative tempo**	f0, 5d, 0e, 08, 19, rr, f7	Relative tempo control by 5% step.
#	**Master Expression**	(f0, 5d, 0e, 08, 1b, ee, f7	Master MIDI Expression. This message is compatible with the all of Oki sound generator LSI. It is independent of “Master volume” but same effect as sub volume controller.
#	**Master Pan**	f0, 5d, 0e, 08, 1c, pp, f7	Master MIDI Panpot. This message is compatible with the all of Oki sound generator LSI. The effect is same as “Master balance” above. The latest message becomes valid.
#	**SG Output bit shift**	f0, 5d, 0e, 08, 21, outp00, bsft, f7	To shift PCM data by the value of “bsft”, for assignd output port by “outp”.
#	**Pile Voice**	f0, 5d, 0e, 08, 7c, dco, onv, f7	To pile same note and increase volume.

(□): <device id>: Any value is accepted. #: Oki Original Exclusive Message

4.1.2 Transpose (f0, 5d, 0e, 08, 10, kkl, kkh, f7)

Command	initial	1	2	3	4	5	6	7	8
Transpose	kk=0	0xf0	0x5d	0x0e	0x08	0x10	kkl	kkh	0xf7

Transpose consists of 8 byte command as above. Transpose effects by a semitone step. Its effective range is from -127 to +127（kkh<<7 +kkl）. 7th bit in “kkh” is a sign bit. After the transpose, when a note No. becomes over the effective range, the note No. is automatically modified as below. When it is over 127, the note No. is modified into 127. When it is under 0, the note No. is modified into 0. “kkh” bit is omissible, then 7th bit in “kkl” becomes a sign bit.

Notice:

This function is same mechanism with transpose register. The latest value is valid. When the transpose function is implemented on the system by register operation, don’t use this exclusive message in a midi file.

4.1.3 Master volume (f0, 5d, 0e, 08, 11, vv, f7)

Command	initial	1	2	3	4	5	6	7
Master volume	vv=100	0xf0	0x5d	0x0e	0x08	0x11	vv	0xf7

Master volume consists of 7 byte command as above. It has same effect with the Master Volume in Universal system exclusive. Those commands are operated exclusively, and latest command is valid.

4.1.4 Synchronous mode set (f0, 5d, 0e, 08, 12, md, d0, d1, f7)

Command	initial	1	2	3	4	5	6	7	8	9
Synchronous mode set	md=2	0xf0	0x5d	0x0e	0x08	0x12	md	0x00	0x00	0xf7

Synchronous mode set consists of 9 byte command as above. It sets synchronous mode between music playback and port operation. “md=2”--- valid, “md≠2”--- invalid.

md	Mode Operation
md≠2	Stop synchronization of MIDI and port control.
md=2	Synchronization of MIDI and port control

4.1.5 Touch correct (f0, 5d, 0e, 08, 13, tt, f7)

Command	Initial	1	2	3	4	5	6	7
Touch correct	tt=0	0xf0	0x5d	0x0e	0x08	0x13	tt	0xf7

Touch correct consists of 7 byte command as above. It modifies velocity value in MIDI files. The value of "tt" is added on velocity value in all note on message.

4.1.6 ADPCM Sync-Play CUE (f0, 5d, 0e, 08, 17, acue, f7)

Command	1	2	3	4	5	6	7
ADPCM Sync-Play CUE	0xf0	0x5d	0x0e	0x08	0x17	acue	0xf7

ADPCM Sync-Play CUE consists of 7 byte command as above. It outputs playback start cue for ADPCM-Player1. When the least significant bit of 6th bit is "1", ADPCM-Player1 starts playback. It is same effect with sync operation which assigned on note No.0 of percussion channel.

4.1.7 Effective Sounds (f0, 5d, 0e, 08, 18, ch, tl, th, f7)

Command	1	2	3	4	5	6	7	8	9
Effective sounds	0xf0	0x5d	0x0e	0x08	0x18	Ch	tl	Th	0xf7

Effective sound consists of 7 byte command as above. It assigns sound effect on selected channel. Select an assigned channel and input 0-15 in "ch". This command and Program change effect exclusively. Regardless of SMF drum channel (Ch.10), any tone or instruments can be assigned on any channel. "th" and "tl" should be set as following table.

th<<7 +tl	Remark
0-127	GM sound set. Equivalent to Bank 0x79.
128-135	GM standard drum set. Equivalent to Bank 0x78.
136-150	Swing'nRinger Original sound set. Equivalent to Bank 0x77.
136	Test Wave: Square Wave 1 (long)
137	Test Wave: Square Wave 1 (short)
138	Test Wave: Square Wave 1 (continuous)
139	Test Wave: Sine Wave 1 (long)
140	Test Wave: Sine Wave 1 (short)
141	Test Wave: Sine Wave 1 (continuous)
142	Test Wave: Loud Square
143	Test Wave: Loud Sine
144	Chinese Musical Instrument: Er hu 1
145	Chinese Musical Instrument: Er hu 2
146	Chinese Musical Instrument: Yang qin
147	Chinese Musical Instrument: Pi pa
148	Chinese Musical Instrument: Sheng
149	Chinese Musical Instrument: Di zi
150	Chinese Musical Instrument: Sona
151 -	Invalid

4.1.8 Relative tempo (f0, 5d, 0e, 08, 19, rr, f7)

Command	initial	1	2	3	4	5	6	7
Relative tempo	rr=0	0xf0	0x5d	0x0e	0x08	0x19	rr	0xf7

Relative tempo message consists of 7 byte command as above. It shifts tempo by 5% step. The sign is set by 6th bit of "rr". The absolute value is set by bit5-0.

Setup Tempo = original tempo * (1+rr * 0.05)
Setting Range: +315% ~ -315%

When setup tempo is calculated fewer than 20 or over 960, the value is automatically modified within the range.

NOTICE:
This function is same mechanism with relative tempo register. The latest value is valid. When the relative tempo function is implemented on the system by register operation, don't use this exclusive message in a midi file.

4.1.9 Master Expression (f0, 5d, 0e, 08, 1b, ee, f7)

Command	initial	1	2	3	4	5	6	7
Master Expression	ee=127	0xf0	0x5d	0x0e	0x08	0x1b	ee	0xf7

It sets substitute volume of cross-channel. Setup range is 0 – 127. It has same kind of function with Master Volume, but independent parameter of it.

4.1.10 Master Pan (f0, 5d, 0e, 08, 1c, pp, f7)

Command	initial	1	2	3	4	5	6	7
Master Pan	pp=64	0xf0	0x5d	0x0e	0x08	0x1c	pp	0xf7

It sets panpot of cross-channel. Setup range is 0 (left) – 64(center) – 127(right). It has same kind of effect with Master balance in Universal system exclusive. Those command effects exclusively, and latest value is applied.

4.1.11 SG Output bit shift (f0, 5d, 0e, 08, 21, outp00, bsft, f7)

Command	initial	1	2	3	4	5	6	7	8
SG Output bit shift	bsft=0	0xf0	0x5d	0x0e	0x08	0x21	0x00	bsft	0xf7

SG Output bit shift enables to shift the bit of PCM output signal from sound generator. The signal amplitude can be shift from 1/64 (minimum) to double (maximum). Please refer to following table for details.

bsft	Amplitude Ratio	Remarks
0	-	Invalid
1	1/64	
2	1/32	
3	1/16	
4	1/8	
5	1/4	
6	1/2	
7	1	Default
8	2	

4.1.12 Pile Voice (f0, 5d, 0e, 08, 7c, dco, onv, f7)

Command	initial	1	2	3	4	5	6	7	8
Pile Voice	dco=1	0xf0	0x5d	0x0e	0x08	0x7c	dco	0x00	0xf7

Pile voice is to increase amplitude of each note, by sacrificing its maximum polyphony. “dco” sets up the assignment of polyphony of each notes. The initial value is 1. The maximum polyphonic numbers of this sound generator is 64. So for example, when “dco”= 2, 3, 4…, the amplitude also becomes 2 times, 3 times, 4 times…, but the maximum poly becomes 32, 21, 16…

4.2 MIDI Reset Specifications

Please refer to below for detail specification of each reset.

Setting Item X:ch0～ch15		default	GM System On	Reset All Control
Control Change (0xBX)	Bank	ch9: 78H others: 79H	ch9: 78H others: 79H	-
	Modulation	0	0	0
	Volume	100	100	-
	Pan	64(center)	64(center)	-
	Expression	127	127	127
	Hold 1 (Sustain)	0	0	0
	RPN	NULL	NULL	NULL
	Pitch Bend Sensitivity	MSB/LSB 02H/00H 256(2 semitone)	MSB/LSB 02H/00H 256(2 semitone)	-
	Fine Tune	40H /00H	40H /00H	-
	Course tune	40H	40H	-
Program Change (0xCX)		0	0	-
After Touch (0xDX)		0	0	0
Pitch Bend (0xEX)		MSB:40H LSB:00H (No change)	MSB:40H LSB:00H ((No change)	MSB:40H LSB:00H ((No change
Exclusive (0xF0)	Master volume	127	-	-
	Master balance	64(center)	-	-
	MIP message	Clear	-	-
Oki Exclusive (0xF0)	Transpose	0	-	-
	Master volume	127	-	-
	Synchronous mode set	Sync On	-	-
	Touch correct	0	-	-
	Effective Sounds	Bank:79Hor78H ProgramNo:0	-	-
	Relative tempo	100%	-	-
	Master Expression	127	-	-
	Master Pan	64(center)	-	-
	SG Output bit shift	5	-	-
	Pile Voice	1	-	-
Meta Message (0xFF)	Tempo	120	-	-
External Parameter	Transpose	0	-	-
	Relative tempo	100%	-	-

4.3 Specification of error processing

Check Item	Condition	Operation
MThd Chunk	When a file header is other than “MThd”.	Error Shutdown.
MThd Chunk Size	When it’s other than 6.	Error Shutdown.
SMF Format	When it’s other than 0.	Error Shutdown.
Track Number	When it’s other than 1.	Error Shutdown.
Time Base	When it’s out of the range from 1 to 0xFFF.	Error Shutdown.
MTrk Chunk	When the character is other than “MTrk”.	Error Shutdown.
Delta Time	When its variable length is more than 5 Byte.	Error Shutdown.
Exclusive Message	When its variable length is more than 5 Byte.	Error Shutdown.

4.4 Effective range for each message

Item List X:ch0～ch15		Melody ch	Percussion ch.	During Playback
Control Change (0xBX)	Bank	Valid	Valid	invalid
	Modulation	Valid	Valid	Valid
	Volume	Valid	Valid	Valid
	Pan	Valid	Valid	Valid
	Expression	Valid	Valid	Valid
	Hold 1 (Sustain)	Valid	Valid	Valid
	RPN	Valid	Valid	Valid
	Pitch bend sensitivity	Valid	Valid	Valid
	Fine Tune	Valid	Valid	Valid
	Course Tune	Valid	invalid	Valid
Program Change (0xCX)		Valid	Valid	invalid
After Touch (0xDX)		Valid	Valid	Valid
Pitch Bend (0xEX)		Valid	Valid	Valid
Exclusive (0xF0)	Master volume	Valid	Valid	Valid
	Master balance	Valid	Valid	Valid
	MIP message	Valid	Valid	-
Oki Exclusive (0xF0)	Transpose	Valid	Valid	Valid
	Master volume	Valid	Valid	Valid
	Synchronous mode set	-	Valid	-
	Touch correct	Valid	Valid	invalid
	Effective Sounds	Valid	Valid	invalid
	Relative tempo	Valid	Valid	Valid
	Master Expression	Valid	Valid	Valid
	Master Pan	Valid	Valid	Valid
	SG Output bit shift	Valid	Valid	Valid
	Pile Voice	Valid	Valid	invalid
MetaMessage (0xFF)	Tempo	-	-	-
External Parameter	Transpose	Valid	invalid	Valid
	Relative tempo	Valid	Valid	Valid

5 Wave-Table Specifications

5.1 Tone Map

Sound is produced even out of recommended range, but sound quality is not guaranteed.

5.1.1 GM Tone Map（BANK79）

Program No	Poly	GM Tone Map	Recommended range
0	1	Acoustic Grand Piano	36-108
1	1	Bright Acoustic Piano	36-108
2	1or2	Electric Grand Piano	36-103
3	2	Honkey-tonk Piano	36-103
4	1	Electric Piano 1	43-96
5	2	Electric Piano 2	48-96
6	2	Harpsichord	36-96
7	1	Clavi	31-91
8	1	Celesta	60-96
9	1or2	Glockenspiel	48-96
10	1	Music Box	60-91
11	2	Vibraphone	48-91
12	1	Marinmba	43-96
13	1	Xylophone	43-96
14	1	Tubular Bells	60-84
15	2	Dulcimer	55-96
16	2	Drawbar Organ	43-96
17	2	Percussive Organ	48-96
18	2	Rock Organ	43-96
19	2	Church Organ	43-100
20	1	Reed Organ	43-84
21	2	Accordion	36-91
22	1	Harmonica	55-84
23	2	Tango Accordion	43-91
24	1	Acoustic Guitar (nylon)	36-84
25	1	Acoustic Guitar (steel)	36-84
26	2	Electric Guitar (jazz)	36-91
27	2	Electric Guitar (clean)	36-91
28	1	Electric Guitar (muted)	31-91
29	2	Overdriven Guitar	36-96
30	2	Distortion Guitar	36-96
31	1	Guitar harmonics	43-91
32	2	Acoustic Bass	24-67
33	1	Electric Bass (finger)	24-60
34	1	Electric Bass (pick)	21-60
35	2	Fretless Bass	24-64
36	1or2	Slap Bass 1	21-60
37	1or2	Slap Bass 2	21-60
38	1	Synth Bass 1	31-72
39	1	Synth Bass 2	28-67
40	1	Violin	55-91
41	1	Viola	48-86
42	1	Cello	36-79
43	1	Contrabass	24-60
44	2	Tremolo Strings	36-96
45	2	Pizzicato Strings	48-91
46	2	Orchestral Harp	43-91
47	1	Timpani	36-67
48	1	String Emsemble 1	36-96
49	1	String Emsemble 2	36-96
50	2	Synth String 1	36-96
51	2	Synth String 2	36-96
52	1	Choir Aahs	55-84
53	2	Voice Oohs	48-84
54	2	Synth Vox	48-91
55	2	Orchestra Hit	43-84
56	1	Trumpet	48-91
57	2	Trombone	36-84
58	2	Tuba	24-72
59	2	Muted Trumpet	48-91
60	1	French Horn	43-84
61	2	Brass Section	36-96
62	2	Synth Brass 1	36-96
63	2	Synth Brass 2	36-96
64	1	Soprano Sax	55-96
65	1	Alto Sax	48-90
66	2	Tenor Sax	43-84
67	2	Baritone Sax	33-64
68	1	Oboe	59-93
69	1	English Horn	48-86
70	1	Bossoon	43-72
71	1	Clarinet	55-91
72	1	Piccolo	72-103
73	1	Flute	60-96
74	1	Recorder	55-88
75	1	Pan Flute	68-95
76	2	Blown Bottle	60-96
77	2	Shakuhachi	55-84
78	1	Whistle	60-96
79	1	Ocarina	60-91
80	2	Lead 1 (square)	36-96
81	2	Lead 2 (sawtooth	36-96
82	2	Lead 3 (calliope)	48-96
83	2	Lead 4 (chiff)	48-91
84	2	Lead 5 (charang)	43-91
85	2	Lead 6 (voice)	55-93
86	2	Lead 7 (fifths)	36-96
87	2	Lead 8 (bass + lead)	36-96
88	2	Pad 1 (new age)	36-96
89	1	Pad 2 (warm)	48-96
90	2	Pad 3 (polysynth)	36-96
91	1	Pad 4 (choir)	48-96
92	2	Pad 5 (bowed)	48-96
93	2	Pad 6 (metallic)	36-85
94	2	Pad 7 (halo)	43-96
95	2	Pad 8 (sweep)	36-96
96	2	Fx1 (rain)	43-84
97	2	Fx2 (soundtrack)	36-84
98	2	Fx3 (crystal)	36-96
99	2	Fx4 (atmosphere)	36-84
100	2	Fx5 (brightness)	48-89
101	2	Fx6 (goblins)	48-83
102	1	Fx7 (echoes)	48-96
103	1	Fx8 (sci-fi)	48-96
104	2	Sitar	43-84
105	2	Banjo	36-84
106	2	Shamisen	43-79
107	2	Koto	48-84
108	2	Kalimba	43-91
109	2	Bag pipe	40-84
110	1	Fiddle	55-91
111	1	Shanai	48-84
112	2	Tinkle Bell	48-91
113	1	Agogo	60-72
114	2	Steel Drums	43-88
115	1	Woodblock	60-72
116	1	Taiko	60-72
117	1	Melodic Tom	60-72
118	1	Synth Drum	48-84
119	1	Reverse Cymbal	60-72
120	2	Guitar Fret Noise	60-72
121	2	Breath Noise	60-72
122	2	Seashore	60-72
123	1	Bird Tweet	60-72
124	2	Telephone Ring	60-72
125	2	Helicopter	60-72
126	2	Applause	60-72
127	2	Gunshot	60-72

5.1.2 Percussion Map (BANK78)

Note No. 0, 96-99, 101, and 127 are assigned for synchronous control.

Note No.	Poly	Percussion name	Default Panpot
0	-	Sync Play Cue	-
1-34	-	(Invalid)	-
35	1	Acoustic Bass Drum	64
36	1	Bass Drum 1	64
37	1	Side Stick	64
38	2	Acoustic Snare	64
39	1	Hand Clap	54
40	2	Electric Snare	64
41	1	Low Floor Tom	34
42	1	Closed Hi-Hat	84
43	1	High Floor Tom	46
44	1	Pedal Hi-Hat	84,
45	1	Low Tom	58
46	1	Open Hi-Hat	84
47	1	Low-Mid Tom	70
48	1	Hi-Mid Tom	82
49	1	Crash Cymbal1	84
50	1	High Tom	94
51	1	Ride Cymbal1	44
52	2	Chinese Cymbal	44
53	1	Ride Bell	44
54	1	Tambourine	74
55	1	Splash Cymba l	54
56	1	Cowbell	84
57	1	Crash Cymba 2	44
58	1	Vibraslap	29
59	1	Ride Cymbal2	44
60	2	Hi Bongo	99
61	1	Low Bongo	99
62	1	Mute Hi Conga	39
63	1	Open Hi Conga	39
64	1	Low Conga	44
65	1	High Timbale	84

Note No	Poly	Percussion Name	Default Panpot
66	1	Low Timbale	84
67	1	High Agogo	29
68	1	Low Agogo	29
69	1	Cabasa	29
70	1	Maracas	24
71	1	Short Whistle	99
72	1	Long Whistle	99
73	1	Short Guiro	94
74	1	Long Guiro	94
75	1	Clavas	84
76	1	Hi Wood Block	99
77	1	Low Wood Block	99
78	1	Mute Cuica	44
79	1	Open Cuica	44
80	1	Mute Triangle	24
81	1	Open Triangle	24
82 - 88	-	(Invalid)	-
89	1	Ban Gu	64
90	1	Hu Yin Luo	64
91	1	Xiao Luo	64
92	1	Xiao Bo	64
93	1	Tang Gu Low	64
94	1	Tang Gu High	64
95	-	(invalid)	-
96	-	LED0 Sync	-
97	-	LED1 Sync	-
98	-	LED2 Sync	-
99	-	LED3 Sync	-
100	-	(Invali)	-
101	-	VIB Sync	-
102-126	-	(Invalid)	-
127	-	Event Sync	-

5.1.3 Swing'nRinger Original Sound Map (BANK77)

GM Standard Drum set is assigned on program No.0 – 7. Test signal is assigned on No. 8 – 15. Chinese traditional instrument is assigned on No.16 – 22. Program No. 23 and above are invalid.

Program No.	Poly	Sound Group	Sound Name	Recommended Range
0		Percussion	GM Standard Drum Set 【BANK78】	
1				
2				
3				
4				
5				
6				
7				
8	1	TEST Wave	Square Wave 1 (long)	53-96
9	1		Square Wave 1 (short)	53-96
10	1		Square Wave 1 (continuous)	53-96
11	1		Sine Wave 1 (long)	53-96
12	1		Sine Wave 1 (short)	53-96
13	1		Sine Wave 1 (continuous)	53-96
14	2		Loud Square	53-96
15	2		Loud Sine	53-96
16	2	Chinese Musical – Instrument	Er hu 1	48-88
17	2		Er hu 2	48-88
18	2		Yang qin	48-96
19	2		Pi pa	43-84
20	1		Sheng	36-84
21	2		Di zi	55-91
22	2		Sona	48-84
23 -		invalid		

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