ML2611 DATASHEET

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General Description

The ML2611 is the Digital to Analog Converter LSI with a high quality 3D surround and Bass enhancement for audio applications. The LSI supports three modes, SRS Headphone, SRS3D Extreme and TruBass with emphasis on low power through a complete hardwired solution. The ML2611 also incorporates stereo headphone amplifiers, stereo speaker amplifiers and 5-band equalizer. Typical applications are mobile phones, portable audio players, Electrical dictionaries, etc.

Features

1) CPU I/F
   I2C slave mode
   - 7bit addressing, address 3bit is fixed at “0011010”
   - Support Standard / Fast mode

2) Serial Audio Interface (SAI)
   - Sampling frequency: 16k, 22.05k, 24k, 32k, 44.1k, 48k Hz
   - Channel data length: 16bit
   - LRCLK positive/negative selectable
   - 1bit delay/Left Justified selectable
   - Slave mode
     MSB first
     BCLK 32clock~128clock
   - Master mode
     32fs/64fs selectable
     MSB first/LSB first selectable

3) Sound Effect
   - 3D surround and TruBass powered by SRS Labs
     SRS headphone: Repositions sound from inside the head to outside the ears
     SRS3D: 3D stereo enhancement from stereo source
     TruBass: Psychoacoustic bass enhancement
   - 5band Equalizer

4) Input Amplifier
   - Stereo line input amprefiers

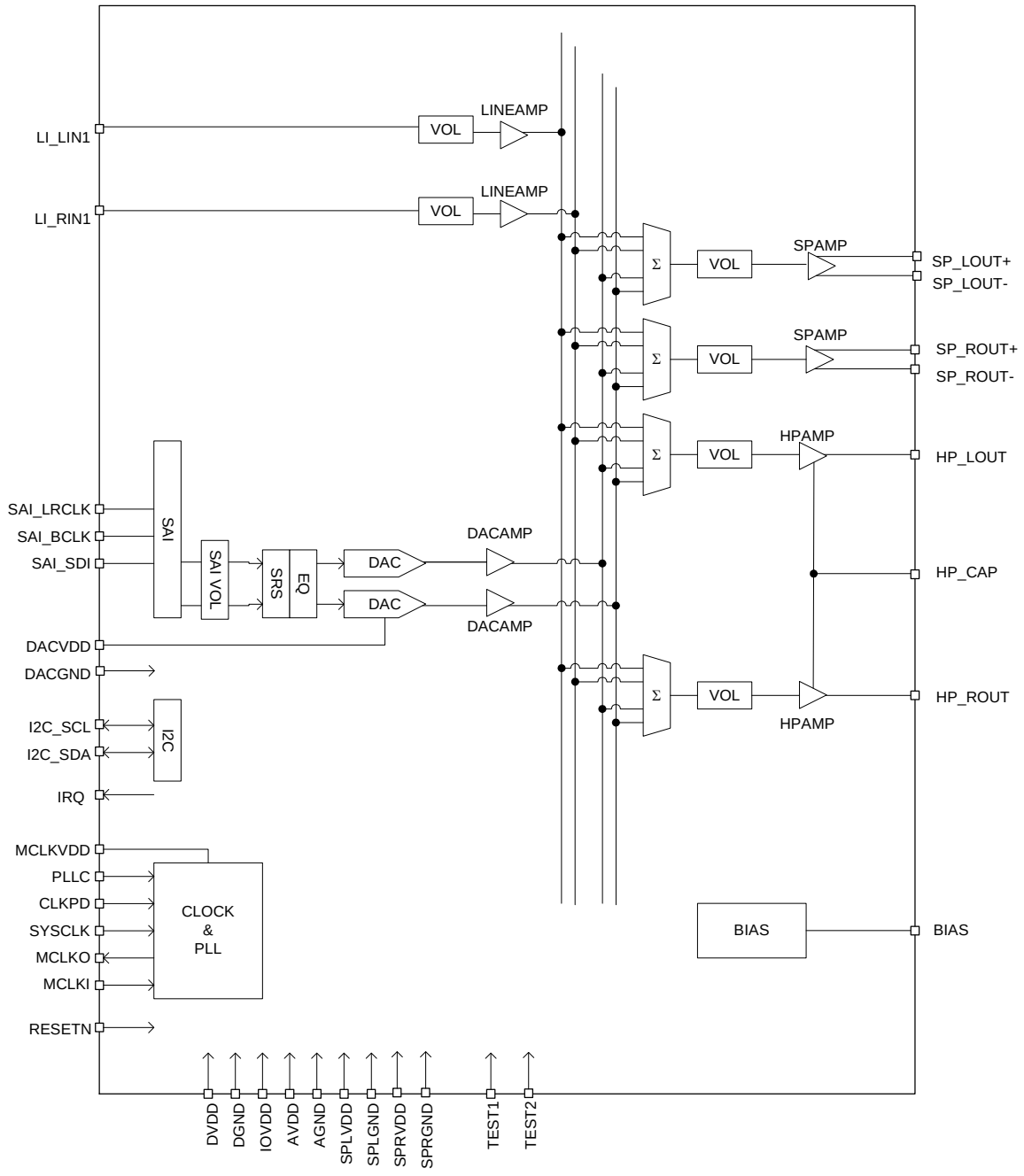
5) DAC
   - 16bit ΔΣ Audio DAC

6) Output Amplifiers
   - Stereo headphone amplifiers
   - Stereo BTL speaker amplifiers

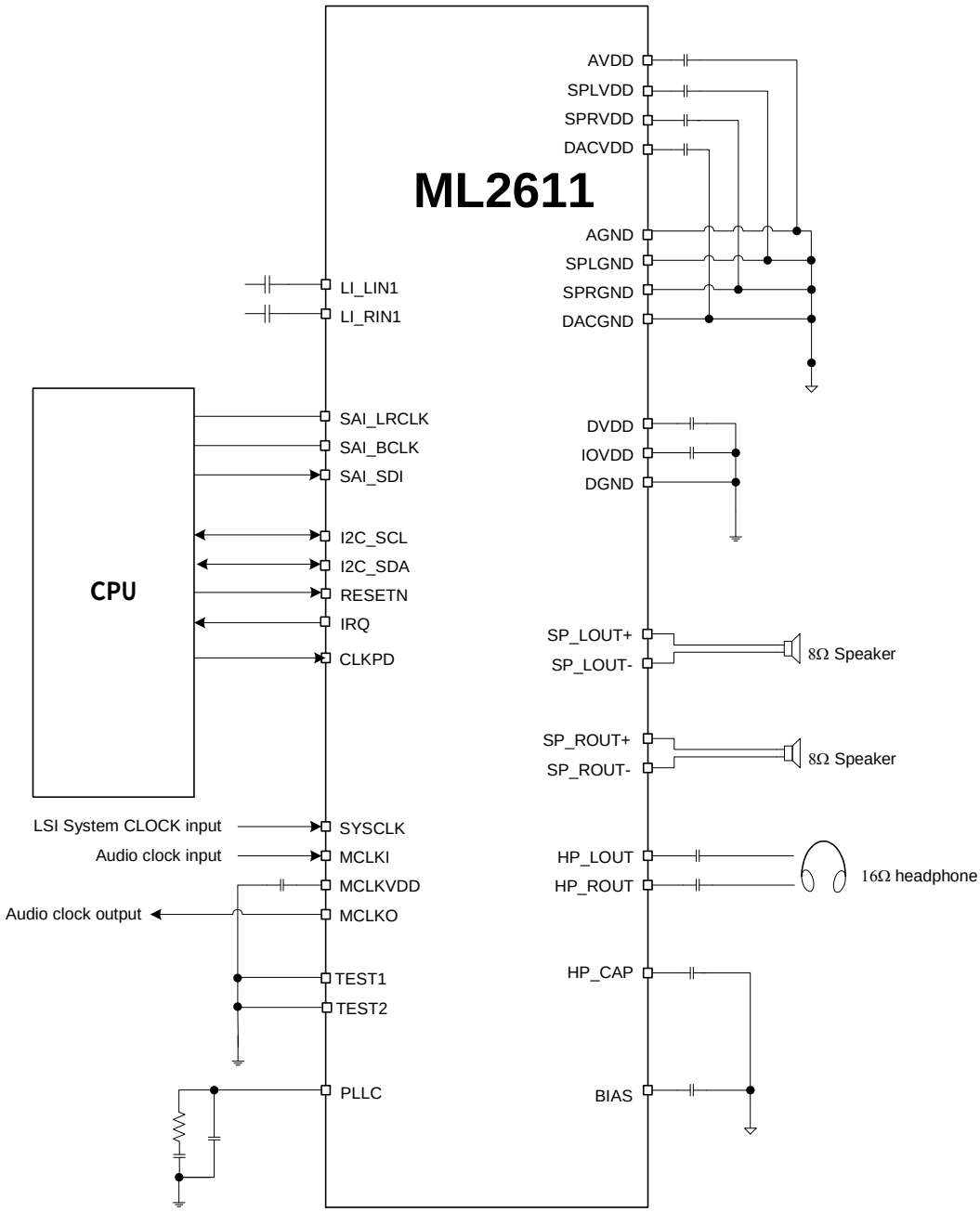
7) Clock
   - 8~20MHz
   - Digital signal or 0.4Vpp sine wave
   - 256fs

8) Package
   Package size: 6.0mm*6.0mm 0.5mm pitch 36pin QFN
   Package size: 3.0mm*3.2mm 0.5mm pitch 36pin WCSP

Block Diagram



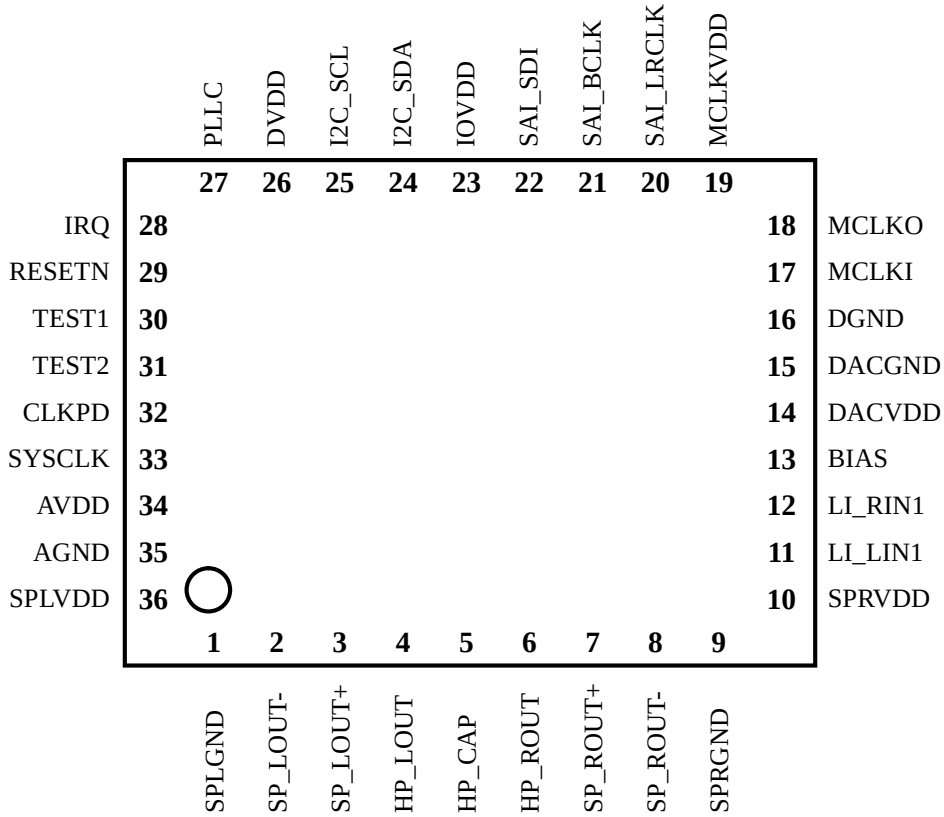
Application Example



Pin Layout

36Pin QFN

Top View

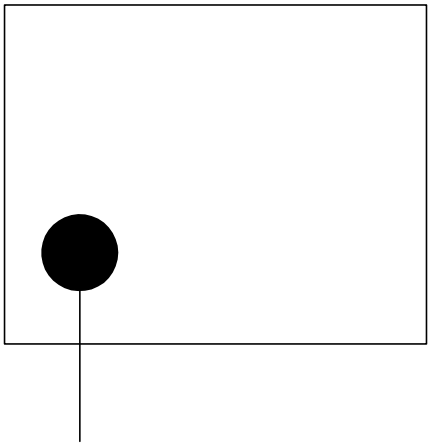


36Pin WCSP

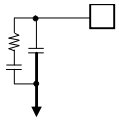
Bottom View

IRQ	DVDD	IOVDD	SAI_SDI	MCLKVDD	MCLKO	**6**
TEST1	PLLC	I2C_SDA	SAI_BCLK	SAI_LRCLK	DGND	**5**
CLKPD	RESETN	I2C_SCL	LI_RIN1	MCLKI	DACGND	**4**
SYSCLK	AVDD	TEST2	HP_CAP	DACVDD	BIAS	**3**
AGND	SPLVDD	SP_LOUT+	SP_ROUT+	SPRVDD	LI_LIN1	**2**
SPLGND	SP_LOUT-	HP_LOUT	HP_ROUT	SP_ROUT-	SPRGND	**1**
F	**E**	**D**	**C**	**B**	**A**	

Top View



Pin Description

Pin No.		Pin Name	IO	Power	Description	Reset state
QFN	WCSP					
8	B1	SP_ROUT-	O	SPRVDD	Speaker – output Right.	Hi-Z
7	C2	SP_ROUT+	O	SPRVDD	Speaker + output Right.	Hi-Z
10	B2	SPRVDD	P	-	Power supply pin for Speaker Right. Please connect 1.0µF capacitor between this pin and SPRGND.	-
9	A1	SPRGND	P	-	Ground pin for Speaker Right.	-
2	E1	SP_LOUT-	O	SPLVDD	Speaker – output Left.	Hi-Z
3	D2	SP_LOUT+	O	SPLVDD	Speaker + output Left.	Hi-Z
36	E2	SPLVDD	P	-	Power supply pin for Speaker Left. Please connect 1.0µF capacitor between this pin and SPLGND.	-
1	F1	SPLGND	P	-	Ground pin for Speaker Left.	-
4	D1	HP_LOUT	O	AVDD	Headphone output Left.	L
6	C1	HP_ROUT	O	AVDD	Headphone output Right.	L
5	C3	HP_CAP	I	DACVDD	Capacitor connect pin for headphone output. Please connect 1.0µF capacitor between this pin and DACGND.	-
11	A2	LI_LIN1	I	AVDD	Left channel line input 1.	-
12	C4	LI_RIN1	I	AVDD	Right channel line input 1.	-
14	B3	DACVDD	P	-	Power supply pin for DAC. Please connect 1.0µF capacitor between this pin and DACGND.	-
15	A4	DACGND	P	-	Ground pin for DAC.	-
34	E3	AVDD	P	-	Power supply pin for Analog. Please connect 1.0µF capacitor between this pin and AGND.	-
35	F2	AGND	P	-	Ground pin for Analog.	-
26	E6	DVDD	P	-	Power supply pin for digital. Please connect 0.1µF capacitor between this pin and DGND.	-
23	D6	IOVDD	P	-	Power supply pin for IO. Please connect 0.1µF capacitor between this pin and DGND.	-
16	A5	DGND	P	-	Ground pin for digital.	-
19	B6	MCLKVDD	P	-	Power supply pin for MCLK. Please connect 0.1µF capacitor between this pin and DGND.	-
33	F3	SYSCLK	I	AVDD	System clock input (8~20MHz).	-
18	A6	MCLKO	O	MCLKVDD	Audio clock (256fs) output.	L
17	B4	MCLKI	I	MCLKVDD	Audio clock (256fs) input.	-
27	E5	PLLC	O	DVDD	Please connect capacitor and resistor on the pin for PLL stable oscillation like following figure. Please see Audio PLL function overview for details.  PLLC pin	L
13	A3	BIAS	O	DACVDD	Capacitor connect pin for Analog reference voltage. Please connect 1.0µF capacitor between this pin and DACGND.	L
29	E4	RESETN	I	IOVDD	Active-low reset input.	-
28	F6	IRQ	O	IOVDD	Interrupt output pin. It outputs “H” level, when the interrupt is generated.	L
32	F4	CLKPD	I	IOVDD	Clock buffer disable control input pin. H: Power down.	-
24	D5	I2C_SDA	IO	IOVDD	I2C bus data input/output.	-(input)
25	D4	I2C_SCL	IO	IOVDD	I2C bus clock input/output.	-(input)
20	B5	SAI_LRCLK	IO	IOVDD	LR clock input/output for SAI.	-(input)
21	C5	SAI_BCLK	IO	IOVDD	Bit clock input/output for SAI.	-(input)
22	C6	SAI_SDI	I	IOVDD	Serial data input for SAI.	-
30	F5	TEST1	I	IOVDD	Test pin. Please connect it to DGND.	(DGND)

31	D3	TEST2	I	IOVDD	Test pin. Please connect it to DGND.	(DGND)

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Digital Supply Voltage	DVDD	-	-0.3~3.5	V
DAC Supply Voltage	DACVDD	-	-0.3~3.5	V
Speaker Right Supply Voltage	SPRVDD	-	-0.3~5.5	V
Speaker Left Supply Voltage	SPLVDD	-	-0.3~5.5	V
Analog Supply Voltage	AVDD	-	-0.3~4.5	V
IO Supply Voltage	IOVDD	-	-0.3~4.5	V
MCLK Supply Voltage	MCLKVDD	-	-0.3~4.5	V
Output Current SP	IOSP		-650 ~ 650(*1)	mA
Output Current HP	IOHP		-250 ~ 250(*2)	mA
Output Current Other	IOO		-8 ~ 8(*3)	mA
Input Voltage	Vin	-	-0.3～IOVDD+0.3	V
Storage Temperature	Tstg	-	-55～+125	°C
Power Dissipation	Pd	Ta=25°C	750	mW

(*1) SPOUT+,SPOUT- pin
(*2) HPOUTL,HPOUTR pin
(*3) except SPOUT+,SPOUT-,HPOUTL,HPOUTR pin
(Output pin includes an IO pin which is in output mode)

Recommended Operating Condition

Parameter	Symbol	Condition	Rating	Unit
Digital Supply Voltage	DVDD	DVDD≦AVDD DVDD=DACVDD	2.25~2.75	V
DAC Supply Voltage	DACVDD	DACVDD≦AVDD DACVDD=DVDD	2.25~2.75	V
Speaker Right Supply Voltage	SPRVDD	-	AVDD~4.5	V
Speaker Left Supply Voltage	SPLVDD	-	AVDD~4.5	V
Analog Supply Voltage	AVDD	-	2.7~3.6	V
IO Supply Voltage	IOVDD	-	1.65~AVDD	V
MCLK Supply Voltage	MCLKVDD	-	1.65~AVDD	V
Operating Temperature	Top	-	-20~+75	°C

Electrical Characteristics

DC Characteristics

(SPLVDD=SPRVDD=2.7~4.5V, DVDD=DACVDD=2.25~2.75V, AVDD= 2.7~3.6V, MCLKVDD=IOVDD=1.65~3.6V, Ta=-20~+75°C, no-load, no-signal)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Related Pin
"H" Input Voltage 1	VIH1	DGND=0V	IOVDD*0.8 MCLKVDD*0.8 AVDD*0.8	-	IOVDD MCLKVDD AVDD	V	*1
"L" Input Voltage1	VIL1	DGND=0V	0	-	IOVDD*0.2 MCLKVDD*0.2 AVDD*0.2	V	
"H" Input Voltage2	VIH2	DGND=0V	IOVDD*0.8	-	3.6	V	*2
"L" Input Voltage2	VIL2	DGND=0V	0	-	IOVDD*0.2	V	
Clock input	Vckin	RFOFF=1 Coupling Capacitor	0.4	-	AVDD*0.8	Vpp	*3
"H" Output Voltage 1	VOH1	IOH=-1mA	IOVDD*0.8 MCLKVDD*0.8	-	-	V	*4
"L" Output Voltage 1	VOL1	IOL=1mA	-	-	IOVDD*0.2 MCLKVDD*0.2	V	
"L" Output Voltage 2	VOL2	IOL=20mA	-	-	IOVDD*0.25	V	*5
"H" Input leakage current	IIH	VI=IOVDD VI=MCLKVDD VI=AVDD	-	-	10	µA	*6
"L" Input leakage current	IIL	VI=DGND VI=AGND	-10	-	-	µA	
Operating Current 1	IDDO1	*7	-	7.5	13	mA	
Operating Current 2	IDDO2	*8	-	7.5	15	mA	
		*8 (LINEAMP/ch)	-	1	-	mA	
		*8 (HPAMP/ch)	-	1	-	mA	
		*8 (DACAMP/ch)	-	1	-	mA	
Operating Current 3	IDDO3	*9	-	3	9	mA	
Operating Current 4	IDDO4	*10	-	3	13	mA	
Standby Current 1	IDDS1	-20~40°C	-	0.2	10	µA	
Standby Current 2	IDDS2	-20~50°C	-	0.5	15	µA	
Standby Current 3	IDDS3	-20~75°C	-	1.5	50	µA	

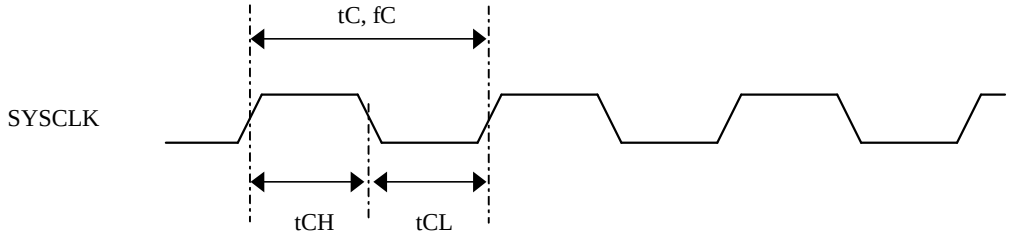
*1 Apply to input or input/output pin except I2C_SCL pin, I2C_SDA pin. Apply to SYSCLK pin (RFOFF="0").
*2 Apply to I2C_SCL pin, I2C_SDA pin.
*3 Apply to SYSCLK pin (RFOFF="1").
*4 Apply to output or input/output pin except I2C_SCL pin, I2C_SDA pin.
*5 Apply to I2C_SCL pin, I2C_SDA pin.
*6 Apply to all input or input/output pin.
*7 Apply to DVDD, DACVDD.
*8 Apply to AVDD.
*9 Apply to MCLKVDD, IOVDD.
*10 Apply to SPLVDD, SPRVDD.
*11 During SYSCLK is stopped. (CLKPD = "H" level)

AC Characteristics

Clock

(SPLVDD=SPRVDD=2.7~4.5V, DVDD=DACVDD=2.25~2.75V, AVDD=2.7~3.6V, MCLKVDD=IOVDD=1.65~3.6V, Ta=-20~+75°C)

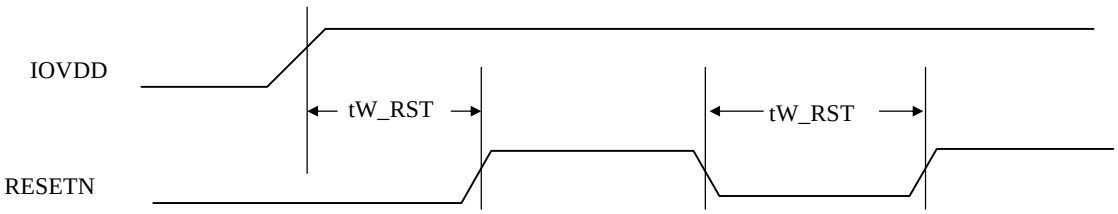
Parameter	Symbol	Min	Max.	Unit
SYSCLK Frequency	fC	8	20	MHz
SYSCLK Period	tC	1/fC	1/fC	ns
SYSCLK H Length	tCH	tC*0.4	–	ns
SYSCLK L Length	tCL	tC*0.4	–	ns



Reset

(SPLVDD=SPRVDD=2.7~4.5V, DVDD=DACVDD=2.25~2.75V, AVDD=2.7~3.6V, MCLKVDD=IOVDD=1.65~3.6V, Ta=-20~+75°C)

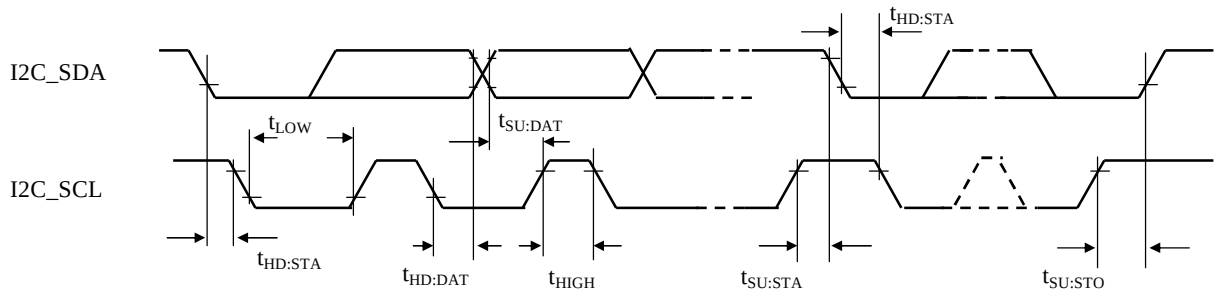
Parameter	Symbol	Min	Max.	Unit
RESETN Pulse Width	tW_RST	5	-	µs



I2C Interface

(SPLVDD=SPRVDD=2.7~4.5V, DVDD=DACVDD=2.25~2.75V, AVDD=2.7~3.6V, MCLKVDD=IOVDD=1.65~3.6V, Ta=-20~+75°C, CL=30pF)

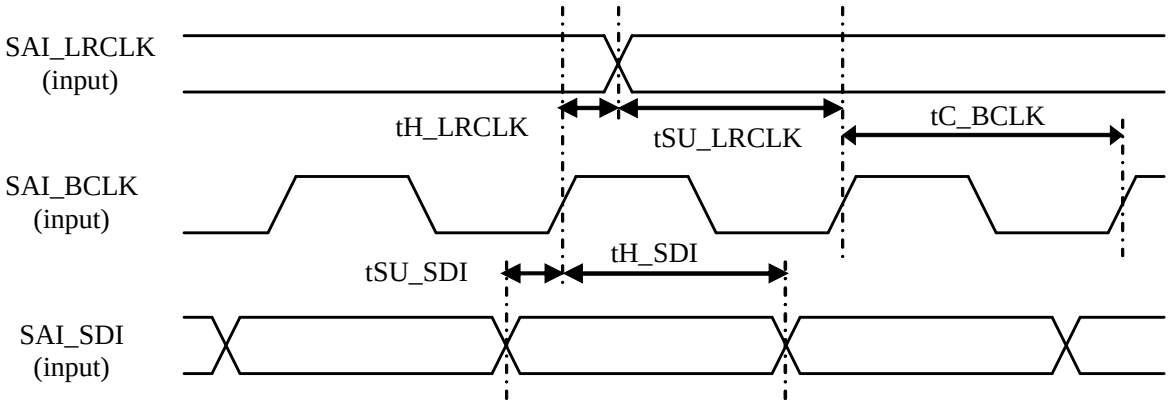
Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max.	Min	Max.	
I2C_SCL Frequency	f_{SCL}	-	100	–	400	kHz
I2C_SCL "L" Length	t_{LOW}	4.7	-	1.3	-	µs
I2C_SCL "H" Length	t_{HIGH}	4.0	-	0.6	-	µs
Hold time under Repeat [Start] Condition	$t_{HD:STA}$	4.0	-	0.6	-	µs
Setup Time under Repeat[Start] Condition	$t_{SU:STA}$	4.0	-	0.6	-	µs
Data Hold Time	$t_{HD:DAT}$	0	-	0	-	µs
Data Setup Time	$t_{SU:DAT}$	250	-	100	-	ns
Setup Time under [Stop] Condition	$t_{SU:STO}$	4.0	-	0.6	-	µs



SAI (Slave)

(SPLVDD=SPRVDD=2.7~4.5V, DVDD=DACVDD=2.25~2.75V, AVDD=2.7~3.6V, MCLKVDD=IOVDD=1.65~3.6V, Ta=-20~+75°C)

Parameter	Symbol	Min	Max.	Unit
SAI_BCLK Period	tC_BCLK	-	128fs	Hz
SAI_LRCLK Hold Time	tH_LRCLK	20	-	ns
SAI_LRCLK Setup Time	tSU_LRCLK	20	-	ns
SAI_SDI Setup Time	tSU_SDI	20	-	ns
SAI_SDI Hold Time	tH_SDI	20	-	ns

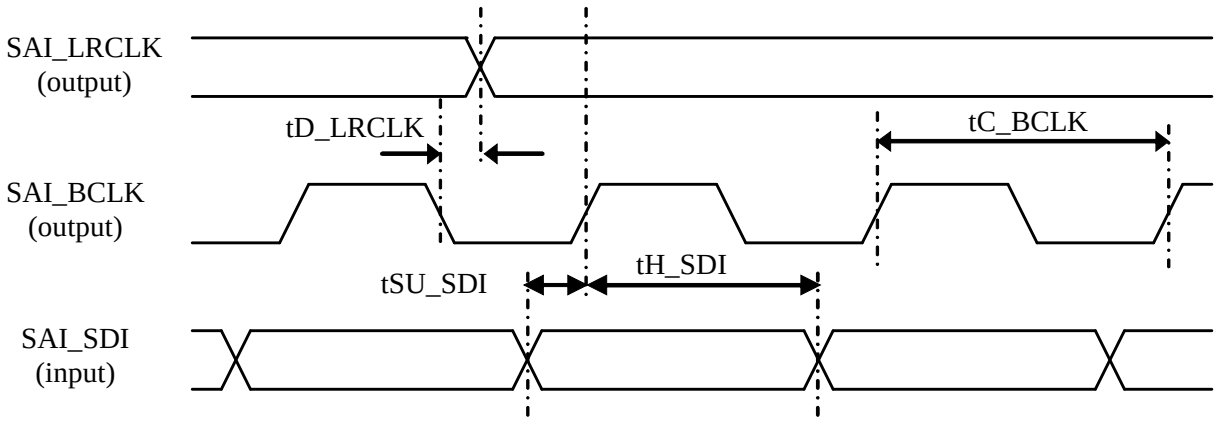


SAI Receive

SAI (Master)

(SPLVDD=SPRVDD=2.7~4.5V, DVDD=DACVDD=2.25~2.75V, AVDD=2.7~3.6V, MCLKVDD=IOVDD=1.65~3.6V, Ta=-20~+75°C, CL=30pF)

Parameter	Symbol	Min	Max.	Unit
SAI_BCLK Period	tC_BCLK	-	64fs	Hz
SAI_LRCLK Delay Time	tD_LRCLK	-	20	ns
SAI_SDI Setup Time	tSU_SDI	50	-	ns
SAI_SDI Hold Time	tH_SDI	0	-	ns

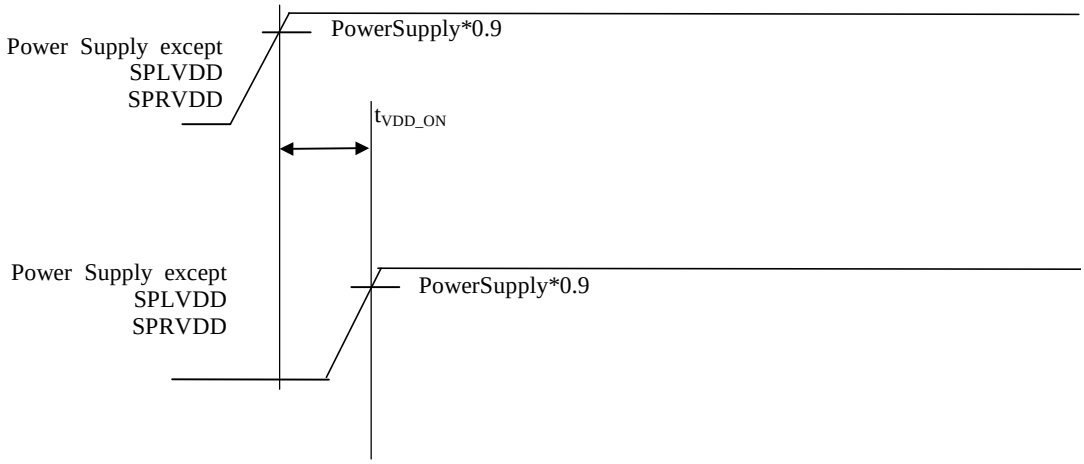


SAI Receive

Power Supply Sequence

Please power on the LSI with all kind of power at the same time. Each power supply should power up in 50ms.

Parameter	Symbol	Min	Typ	Max	Unit
Power On Delay Time	t_{VDD_ON}	0	—	50	ms



Please power off the LSI with all kind of power at the same time(except SPLVDD/SPRVDD). Each power supply should power down in 50ms.

Please keep all power supply in the ON state or the OFF state(except SPLVDD/SPRVDD). Please avoide partial ON or partial OFF status.

Analog Characteristics

Speaker amplifier

SPLVDD=SPRVDD=3V, DACVDD=2.5V, Ta=25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Load Impedance	Rload		8	-	-	Ω
Playable Maximum Frequency	Fmax	Rload=8Ω	20	-	-	kHz

Headphone amplifier

SPLVDD=SPRVDD=3V, DACVDD=2.5V, Ta=25°C C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Load Impedance	Rload		16	-	-	Ω
Playable Maximum Frequency	Fmax	Rload=16Ω	20	-	-	kHz

DAC

AVDD=3V, DACVDD=2.5V, Ta=25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resolution	DAb		-	16	-	bit
S/N	DAsnd1		-	90	-	dB

Line input

AVDD=3V, DACVDD=2.5V, Ta=25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input resistance	Ri		-	30	-	kΩ

Power Derating Curves

Conditions

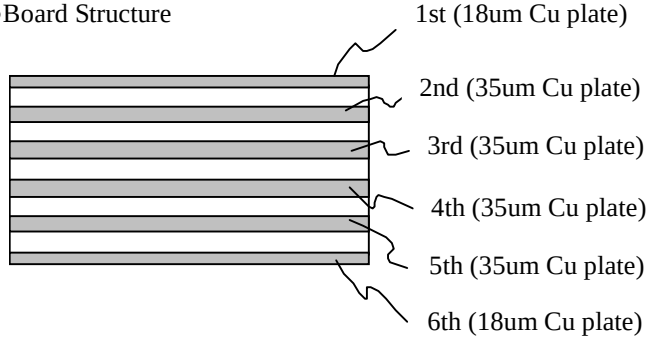
●Board size：70mm*35mm*1.0mm

●Layer：6

●Cooling condition：0m/s

●Simulator：Flotherm

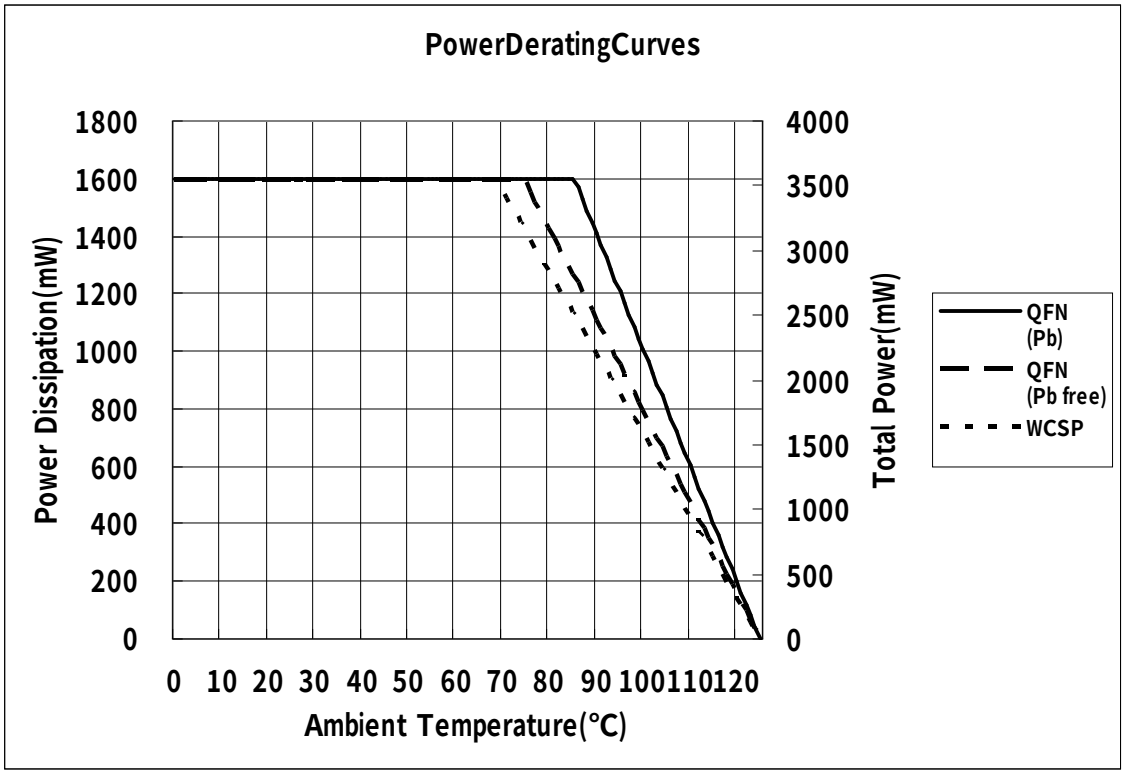
●Board Structure



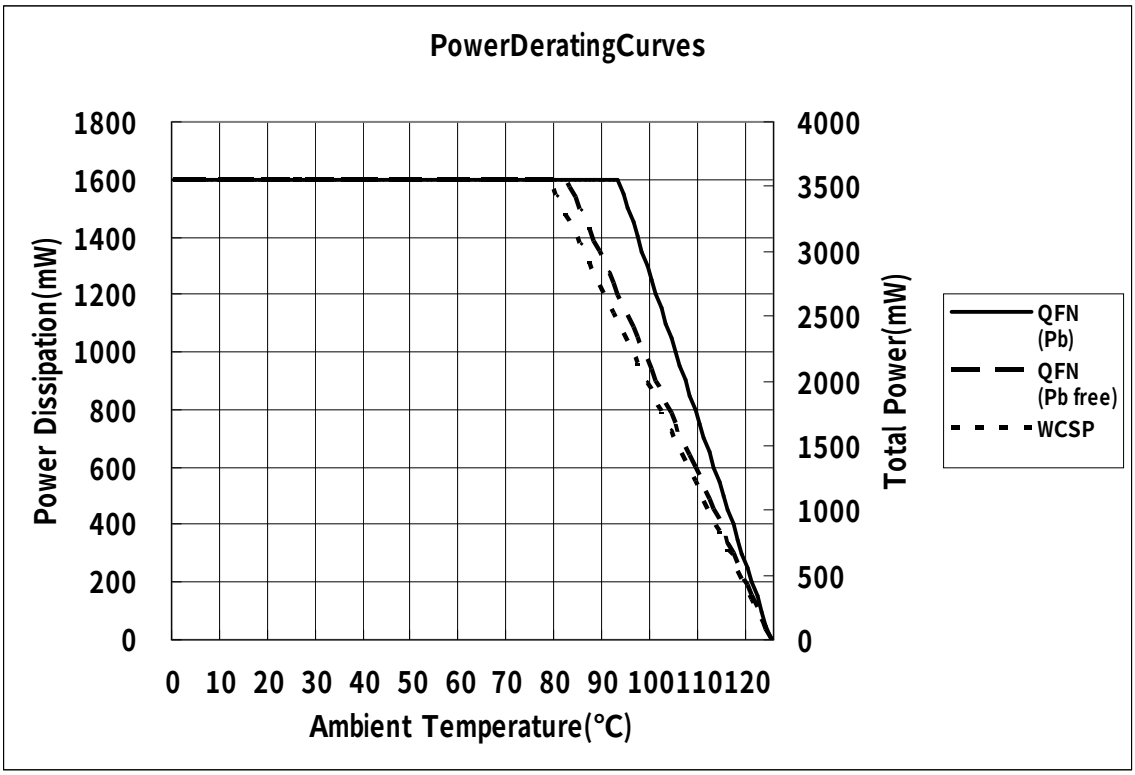
●Board Metal Density:

Simulation Condition						
Board Metal Density	1st	2nd	3rd	4th	5th	6th
50%	50%	-	-	-	-	-
75%	75%	-	-	-	-	-
100%	50%	50%	-	-	-	-
150%	50%	100%	-	-	-	-
200%	50%	100%	50%	-	-	-
250%	50%	100%	100%	-	-	-
350%	50%	100%	100%	100%	-	-
450%	50%	100%	100%	100%	100%	-
500%	50%	100%	100%	100%	100%	50%

PowerDeratingCurves(board 100%)



PowerDeratingCurves(board 200%)



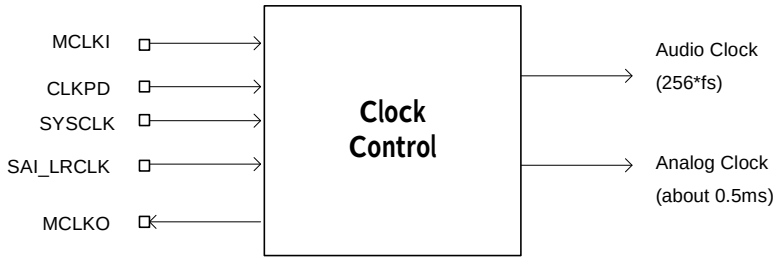
Power Dissipation：power dissipation inside ML2611
Total Power：power dissipation inside ML2611 and speaker power dissipation

Functional Description

Clock

Clock control function overview

Following figure shows the functional block diagram related to the clock control.



Internal Clock overview

1. Audio Clock

   Fuctional block to be used：SAI, SAI Volume, Sound Effecters, DAC

   Setting registers：Clock Select Register, Audio PLL Times 1, 2 Register, Audio PLL Div Register, Audio PLL Timer register

2. Analog Clock

   Fuctional block to be used： Line Input Amplifier, Headphone Amplifire, Speaker Amplifire

   Setting registers：Analog Input Clock Setting Register, Stereo Headphone Amp Timer Register

Note:

Analog clock frequency should be adjust to 2k Hz by setting PC and ADIVA

Analog clock frequency = = (fCLOCK / (PC+1)) ／2^ADIV (^: power)

fCLOCK: Input clock frequency for SYSCLK pin pin

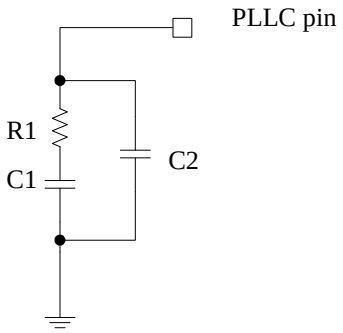
PC: PC[6:0] value

ADIV: ADIV[3:0] value

Audio PLL function overview

External circuit diagram of PLLC pin

Please configure following circuit on PLLC pin



The value of the capacitor and register is altered according to register value of PLLSRC[1:0] bit. Please see following table for each value.

	PLLSRC[1:0] = x1	PLLSRC[1:0] = 10
R1	2.2kΩ	2.7kΩ
C1	100nF	330nF
C2	4.7nF	10nF

PLL operation details

PLL output frequency is set by PLLNVAL bits of Audio PLL Times1 Register, PLLMVAL bits of Audio PLL Times2 Register and PLLDVAL bits of Audio PLL Div Register. Following is the output frequency formula.

1.NVAL=0

PLL output frequency(Hz)=PLL input frequency* (PLLMVAL+2) /((PLLNVAL+1)*(PLLDVAL+2)*2)

Note)

PLL input frequency * (PLLMVAL+2) /(PLLNVAL+1) =158MHz~173MHz

2.NVAL≠0

PLL output frequency(Hz)=PLL input frequency* (PLLMVAL+2) /((PLLNVAL+2)*(PLLDVAL+2)*2)

Note)

PLLinput frequency * (PLLMVAL+2) /(PLLNVAL+2) =158MHz~173MHz

PLL condition setting (changing) sequence

1. Disable PLL by setting PLLEN bit of Sound Path Control Register to “0”.
2. Set PLL output to 256fs clock by setting CLK256SEL[2:0] of Clock Select Register to “xx1”.
3. Set PLLNVAL, PLLMVAL and PLLDVAL of Audio Times Registers.
4. Set PLL wake up time by setting Audio PLL Timer Register.
5. Set IRQ polarity by setting ISS bit of Interrupt Polarity Register.
6. Set PLLEN bit of Sound Path Control Register to “1”.
7. Enable AMP and PLL interrupt by setting APENB bit of Interrupt Enable Register to “1”.
8. Wait for the interrupt caused by PLL start.

Setting example of Audio Times Registers

SAI is in use of master mode, and frequency of system clock is 13MHz:

Sampling frequency	fs	16	22.05	24	32	44.1	48	kHz
Output frequency	FOUT	256fs	256fs	256fs	256fs	256fs	256fs	
		4.096	5.6448	6.144	8.192	11.2896	12.288	MHz
Select audio clock clk256fs	CLK256SEL	x10	x10	x10	xx1	xx1	xx1	*1
Setting value of Counter_N	NVAL	129	112	118	129	112	118	*2

Setting value of Counter_M	MVAL	1649	1384	1586	1649	1384	1586	*2
Setting value of Counter_D	DVAL	8	5	5	8	5	5	*2
Error of output frequency	-	-1.9	-11.2	7.8	-1.9	-11.2	7.8	ppm

SAI is in use of master mode, and frequency of system clock is 19.2MHz:

Sampling frequency	fs	16	22.05	24	32	44.1	48	kHz
Output frequency	FOUT	256fs	256fs	256fs	256fs	256fs	256fs	
		4.096	5.6448	6.144	8.192	11.2896	12.288	MHz
Select audio clock clk256fs	CLK256SEL	x10	x10	x10	xx1	xx1	xx1	*1
Setting value of Counter_N	NVAL	148	123	148	148	123	148	*2
Setting value of Counter_M	MVAL	1278	1027	1342	1278	1027	1342	*2
Setting value of Counter_D	DVAL	8	5	5	8	5	5	*2
Error of output frequency	-	0.0	0.0	0.0	0.0	0.0	0.0	ppm

SAI is in use of slave mode:

Sampling frequency	fs	16	22.05	24	32	44.1	48	kHz
Output frequency	FOUT	256fs	256fs	256fs	256fs	256fs	256fs	
		4.096	5.6448	6.144	8.192	11.2896	12.288	MHz
Select audio clock clk256fs	CLK256SEL	xx1	xx1	xx1	xx1	xx1	xx1	*1
Setting value of Counter_N	NVAL	0	0	0	0	0	0	*2
Setting value of Counter_M	MVAL	10238	7166	7166	5118	3582	3582	*2
Setting value of Counter_D	DVAL	18	12	12	8	5	5	*2
Error of output frequency	-	0.0	0.0	0.0	0.0	0.0	0.0	ppm

*1 binary number
*2 decimal number

Input clock amplitude
Input clock amplitude is permitted from 0.4Vpp to Full Swing. Conditions are as follows.:
If the High level and Low level of the clock amplitude is not low voltage(0.4 to 0.8AVDD Vpp), there is no need to connect a coupling capacitor to the clock input pin.
If the clock amplitude is low voltage, the ML2611 needs its clock input via a coupling capacitor.
If the amplitude of the clock is low voltage, the RFOFF bit should be set to '0' in the Clock Feedback Resistor Control Register.

The formura and the table below show the relationship between the coupling capacitor value and the stabilizing time (the time from the clock start to the clock stable) of the on-board clock.
Recommended coupling capacitor value is 100pF.

CLOCK stabilizing time(s) = (Coupling Capacitor) * 5MΩ

Coupling Capacitor	CLOCK stabilizing time	Register setting

no	0	RFOFF="1"
100pF	0.5ms	RFOFF="0"
1000pF	5ms	RFOFF="0"
0.01uF	50ms	RFOFF="0"
0.1uF	500ms	RFOFF="0"

SYSCLK Stop

When the following amplifires are operated and other peripherals are stoped, power consumption will be reduced by stopping SYSCLK.

- Line input amplifiers
- Speaker output amplifiers
- Headphont amplifiers

SYSCLK Stop operation sequence

1. Enable AMP and PLL interrupt by setting APENB bit of Interrupt Enable Register to “1”.
2. Set the volume of applicable amprefire.
3. Enable applicable amplifire by setting Sound Path Control Register, Stereo Headphone Amp Input Select Register or Speaker Amp Input Select Register.
4. Wait for the interrupt that is confirmed by APRP bit of Interrupt Status Register or IRQ pin.
5. Disable SAI, Sound effecters and DAC by clearing Sound Pass Control registers.
6. Set PLLEN bit of Sound Path Control Register to “0”.
7. Wait SYSCLK 10 pulse (125ns at 8MHz, 500ns at 20MHz) after I2C STOP condition is ready.
8. Stop SYSCLK by setting CLKPD pin at “H” level.

When SYSCLK stops, I2C communication is disabled. Stop the amplifiers or change the register value after SYSCLK is enabled by setting CLKPD pin input to “L” level.

- Related Register
  Clock Select Register
  MCLKO Output Control Register
  Clock Feedback Resistor Control Register
  Audio PLL Times 1 Register
  Audio PLL Times 2 Register
  Audio PLL Timer Register
  Audio PLL Div Register
  Sound Path Control Register
  Analog Input Clock Setting Register
  Interrupt Enable Register
  Interrupt Polarity Register

Reset

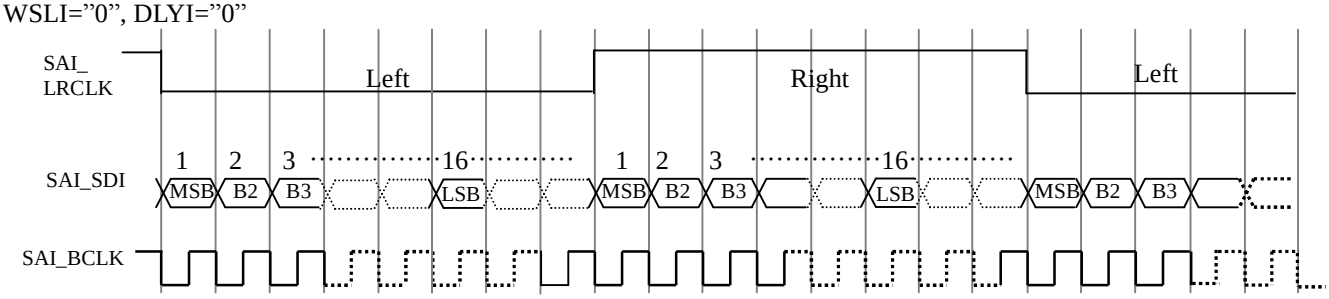
Since an anti-noise filter is embedded within the LSI in order to avoid the wrong resetting, please input RESET signal with at least a 5µs pulse width.

When the RESET signal is asserted during clock stop, negate RESET signal after clock stavilizing time.

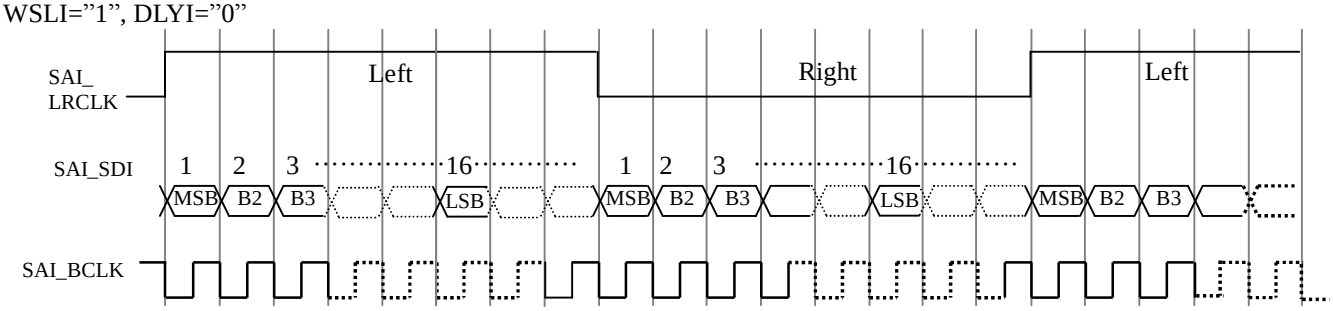
SAI (Serial Audio Interface)

The LSI supports four SAI formats.

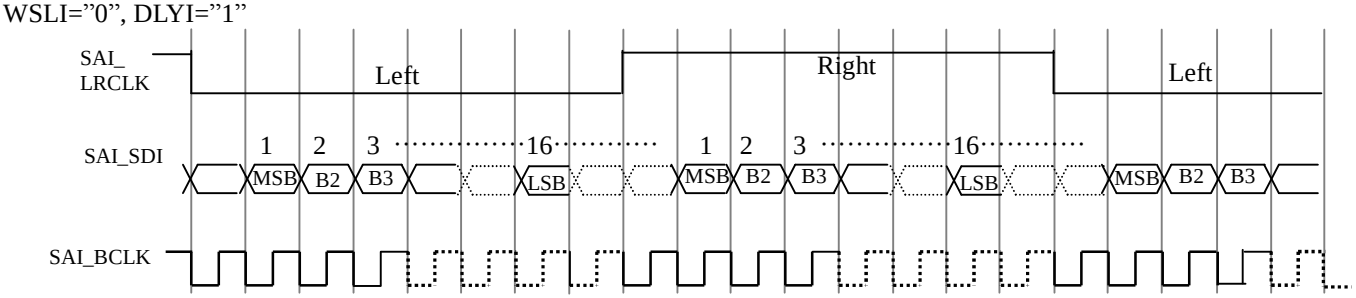
WSLI=”0”, DLYI=”0”



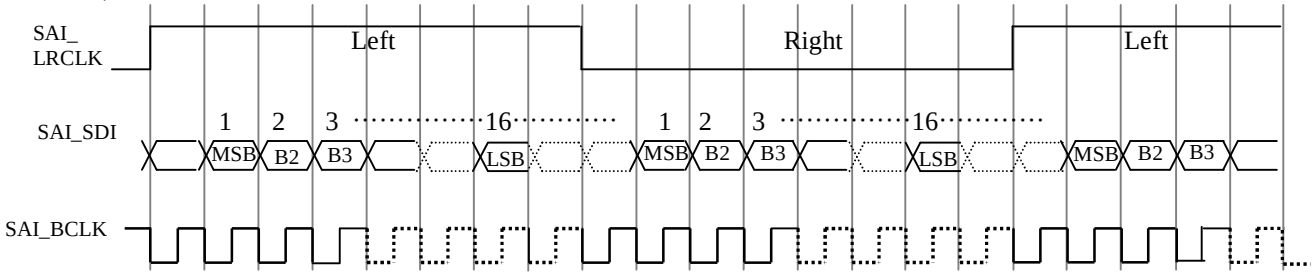
WSLI=”1”, DLYI=”0”



WSLI=”0”, DLYI=”1”



WSLI=”1”, DLYI=”1”



- Related Register
  SAI Control 1 Register
  SAI Control 2 Register

I2C Interface

The ML2611 has the serial interface, which complies with I2C bus standards. The ML2611 operates as an I2C slave device. The ML2611 address is fixed at “0011010”.

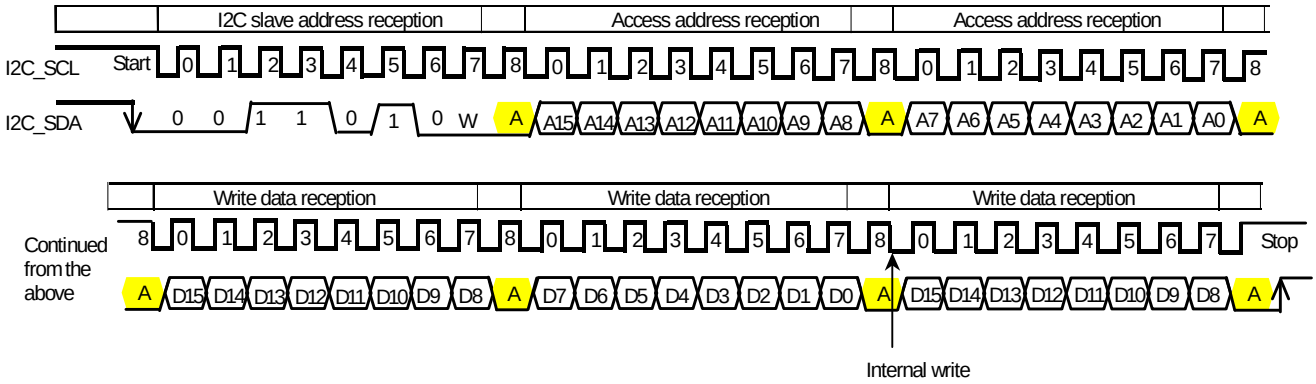
- I2C format

The followings are the I2C protocol of ML2611.
Write(MSB first)
Start condition(Set I2C_SDA level from “H” to “L” during I2C_SCL=”H”)
I2C Slave Address(0011010)＋W(0) (8bit)
Write Address (16bit)
Write Data (16bit)
…
Stop condition(Set I2C_SDA level from “L” to “H” during I2C_SCL=”H”)
Read(MSB first)
Start condition
I2C Slave Address(0011010)＋W(0) (8bit)
Read Address (16bit)
(Stop condition) Start condition
I2C Slave Address(0011010)＋R(1) (8bit)
Read Data (16bit)

The following shows the I2C wave form of ML2611.
The tellow gridding shows that slave device(ML2611) drives I2C bus.
The symbol in the wave form means as following table.

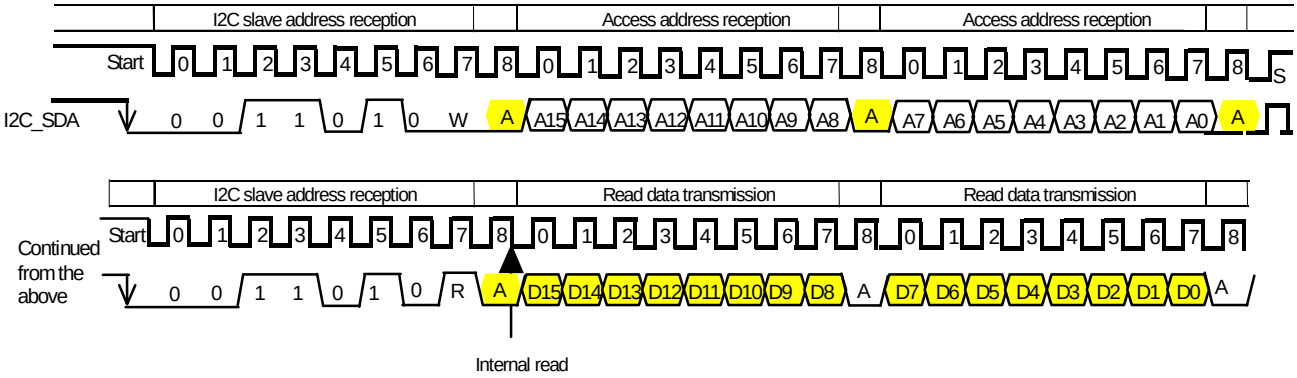
Symbol	Description
W/R	0: Write 1: Read
A	0: ACK(Acknowledge) 1: NAK(Not Acknowledge)
A[15-0]	Access Address (16bit)
D[15-0]	Access Data(16bit)

Write



In case there is no Stop or Start condition after internal register is written (Above figure: Internal Write), the slave device(ML2611) becomes continuous write mode and the next received 16 bits of data will be written into the internal register addressed by incremented by two to the current address.

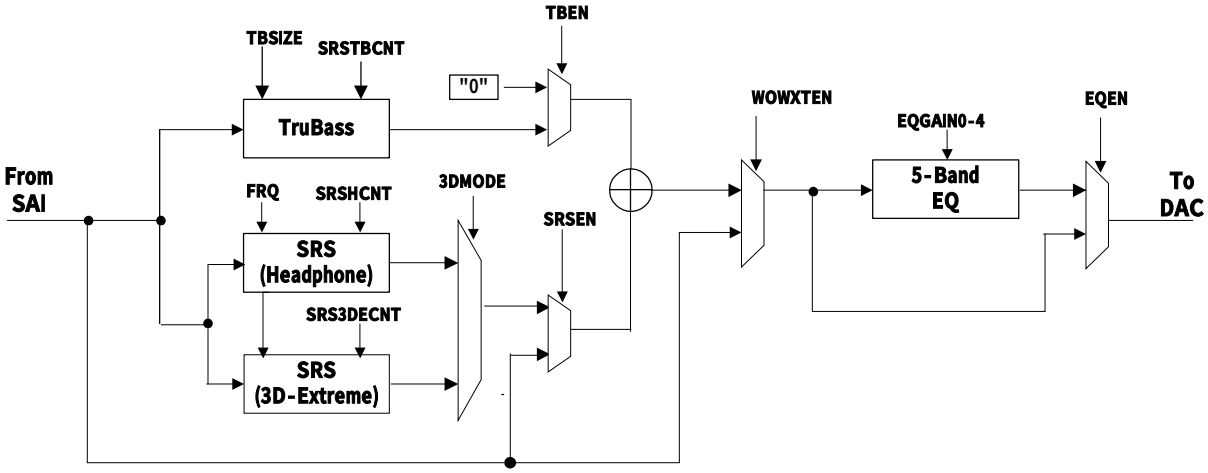
Read



If the Master device return ACK(acknowledge) after the 16 bit data transferred from the ML2611, The ML2611 becomes continuous read mode. The next received 16 bits of data will be red from the internal register addressed by incremented by two to the current address.

Sound Effecters

Sound effecters function overview
Sound effecters functional block diagram



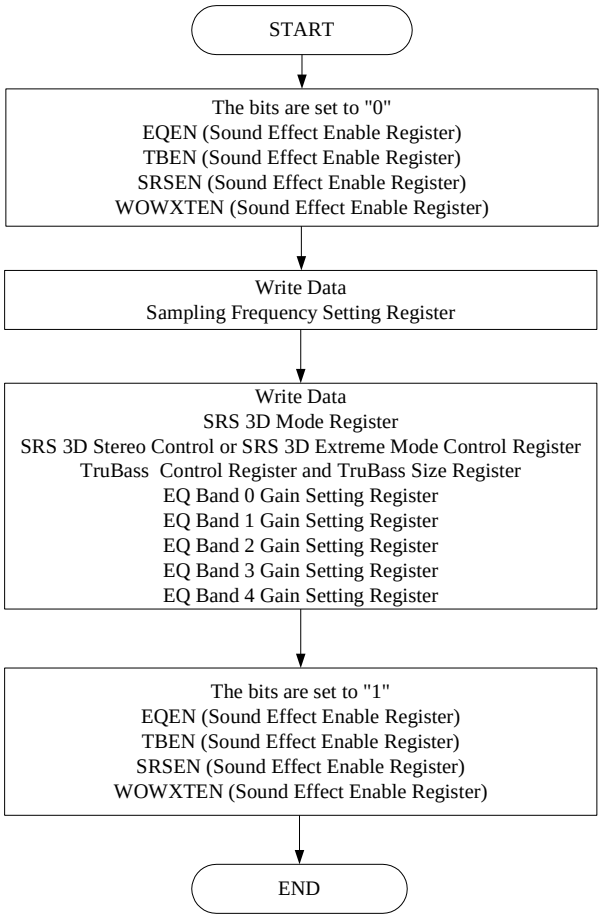
The ML2611 provides high quality audio enhancement technologies powered by SRS Labs and 5-band equalizer. The ML2611 incorporates three technologies, SRS Headphone, SRS3D extreme mode and TruBass. SRS Headphone is 3D surround technology optimized for headphones, SRS3D extreme mode is extremely wide stereo imaging technology optimized for closely spaced speakers. TruBass lowers the perceived bass response well beyond the low frequency limitations of the drivers.

When the SRS labs audio enhancement technologies (SRSEN) is enabled please consider the sound volume. If the input volume to the ML2611 is high, the output sound with the SRSEN might be distorted. In such case, please reduce the audio gain before inputting to the ML2611. Regarding the attenuation value, please determine it by system evaluation.

To disable SRS labs audio enhancement technologies and/or 5-band equalizer, the ML2611 support “Bypass mode”.

Note
SRS3D extreme mode is not recommended for driving headphones.
SRS Headphone is not recommended for driving speakers.

Set Sound Effecters
To use Sound Effecters, control the ML2611 as flowchart bellow.



- Related register
  - Sound Effect Enable register
  - Sampling Frequency Setting register
  - SRS3D Mode register
  - SRS3D Stereo Control register
  - SRS3D Extreme Mode Control register
  - EQ Band 0 Gain Setting register
  - EQ Band 1 Gain Setting register
  - EQ Band 2 Gain Setting register
  - EQ Band 3 Gain Setting register
  - EQ Band 4 Gain Setting register
  - TruBass Control register
  - TruBass Size register

Input/Output Amplifiers and DAC

Start up sequence

To start up the amplifires and DAC, enable Input Amplifires(Stereo Line Input Amplifire) or DAC firtst, and then enable Output Amplifires(Headphone Amplifire or Speaker Amplifire). Output Amplifires cannot be enabled untill Input Amplifires or DAC is enabled. To enable Onput Amplifire, Interrupt generation caused by Input Amplifire or DAC is not nessesary.

Note
1. To operate both Speaker amplifier and headphone amplifier at same time is inhibited.
2. Please refer Stereo Headphone Amp Input Select register description when operating enable headphone.

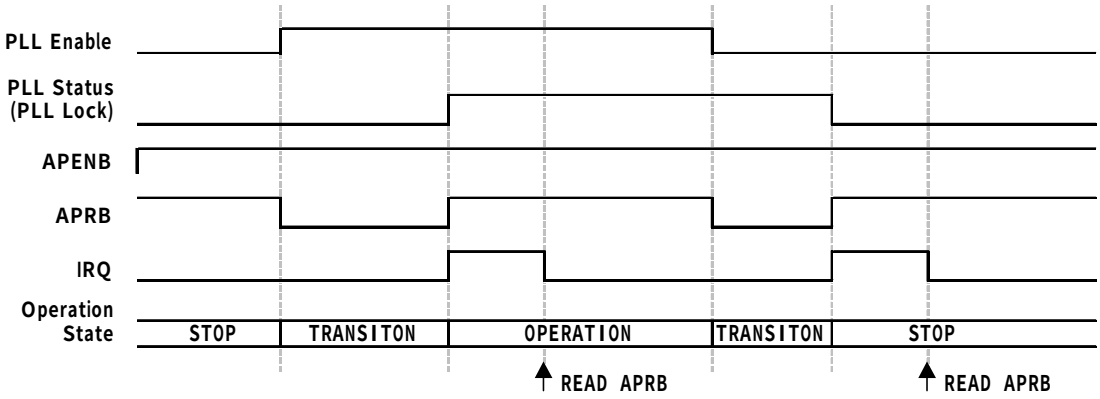
Shut down sequence

To stop the amplifires and DAC, disable Output Amprefires first and then disable Input Amplifire or DAC. If input Amplifire or DAC is disabled first, the pop noise may generated.

Interrupt

Interrupt function overview

To enable AMP, PLL Interrupt, set APENB bit of the Interrupt Enable Register to “1”. When actual operation status of Amplifire and/or PLL much the related register setting,(i.e. there is time difference between setting the resisters to start condition of PLL and actual PLL circuit operation) IRQ pin becomes “H” level and APRB bit of Interrupt Status Register is set to “1”.



Register Map

Note 1: 0xXXXX, 0xXX represents a hexadecimal number

Note 2: "-" indicates a reserved bit. They return "0" for reads. Always write "0" to the bit. If a"1"is written to this bit, the operations cannot be guaranteed.

Address	Access	b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00	Name
Clock, Reset Control Registers																		
0x0004	R/W	-	-	-	-	-	-	-	-	-	-	-	PLLSRC[1:0]		CLK256SEL[2:0]			Clock Select
		-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	
0x0006	R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	MCLKOEN	MCLKO Output Control
		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	
0x0008	R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RFOFF	Clock Feedback Resistor Control
		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	
0x000A	R/W	-	-	-	-	-	-	-	-	PLLNVAL[7:0]								Audio PLL Times 1
		-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	
0x000C	R/W	PLLMVAL[15:0]																Audio PLL Times 2
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
0x000E	R/W	-	-	-	-	-	-	-	PLLOEN	PLLDVAL[7:0]								Audio PLL Div
		-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	
0x0018	R/W	-	-	-	-	-	-	-	-	PLLTMR[7:0]								Audio PLL Timer
		-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	
0x0020	W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SOFTRST	Software Reset
		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	
Sound Path Control Registers																		
0x0100	R/W	-	SAIREN	-	PLLEN	DACEN	-	-	-	-	-	LIL1EN	-	-	-	-	LIR1EN	Sound Path Control
		-	0	-	0	0	-	-	-	-	-	0	-	-	-	-	0	
0x0102	R/W	-	-	-	-	-	-	-	-	-	-	-	-	EQEN	TBEN	SRSEN	WOWXTEN	Sound Effect Enable
		-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	
0x01A2	R/W	-	DMX_VOLSAI_L[6:0]							-	DMX_VOLSAI_R[6:0]							Digital Mixer SAI Volume
		-	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0	
Sound Effect Control Registers																		
0x01B6	R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	FRQ[2:0]			Sampling Frequency Setting
		-	-	-	-	-	-	-	-	-	-	-	-	-	0	1	0	
0x01B0	R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	3DMODE	SRS 3D Mode
		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	
0x01B2	R/W	-	-	-	-	-	-	-	-	-	SRSHCNT[6:0]							SRS Headphone Control
		-	-	-	-	-	-	-	-	-	1	1	0	0	1	1	0	
0x01B4	R/W	-	-	-	-	-	-	-	-	-	SRS3DECNT[6:0]							SRS 3D Extreme Control
		-	-	-	-	-	-	-	-	-	1	1	0	0	1	1	0	
0x01B8	R/W	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TBSIZE	SRS TruBass Size
		-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	
0x01BA	R/W	-	-	-	-	-	-	-	-	-	SRSTBCNT[6:0]							SRS TruBass

		-	-	-	-	-	-	-	-	-	1	1	0	0	1	1	0	Control
0x01C2	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	EQGAIN0[4:0] 0	1	0	1	0	EQ Band 0 Gain Setting
0x01C4	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	EQGAIN1[4:0] 0	1	0	1	0	EQ Band 1 Gain Setting
0x01C6	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	EQGAIN2[4:0] 0	1	0	1	0	EQ Band 2 Gain Setting
0x01C8	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	EQGAIN3[4:0] 0	1	0	1	0	EQ Band 3 Gain Setting
0x01CA	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	EQGAIN4[4:0] 0	1	0	1	0	EQ Band 4 Gain Setting
SAI Interface Control Registers																		
0x0190	R/W	- -	- -	- -	- -	MSBI 0	ISSCKI 0	AFOI[1:0] 0	0	DLYI 0	WSLI 0	- -	- -	- -	- -	- -	- -	SAI Control 1
0x0192	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	MST 1	SAI Control 2
Input/Output Amplifiers Control Registers																		
0x0110	R/W	- -	- -	- -	- -	- -				- -	- -	- -	- -	LITIMER[3:0] 0	1	1	0	Stereo Line Input Amp Timer
0x0112	R/W	- -	PC[6:0] 0	0	0	0	0	0	0	- -	- -	- -	- -	ADIV[3:0] 0	0	0	0	Analog Input Clock Setting
0x0114	R/W	- -	- -	LIV1[5:0] 0	0	0	0	0	0	- -	- -	0	0	RIV1[5:0] 0	0	0	0	Stereo Line Input Ch1 Volume
0x011E	R	- -	- -	- -	- -	- -	- -	- -	LST0 0	- -	- -	- -	- -	- -	- -	-	RST0 0	Stereo Line Input Status
0x0150	R/W	- -	- -	- -	- -	HLDR 0	HLDL 0	HLLR 0	HLLL 0	- -	- -	- -	- -	HRDR 0	HRDL 0	HRLR 0	HRLL 0	Stereo Headphone Amp Input Select
0x0152	R/W	- -	- -	HLV[5:0] 0	0	0	0	0	0	- -	- -	0	0	HRV[5:0] 0	0	0	0	Stereo Headphone Amp Volume
0x0154	R/W	- -	- -	- -	- -	- -	- -	- -	HLG 0	- -	- -	- -	- -	- -	- -	- -	HRG 0	Stereo Headphone Amp Gain Control
0x0156	R	- -	- -	- -	- -	HLSDR 0	HLSDL 0	HLSLR 0	HLSLL 0	- -	- -	- -	- -	HRSDR 0	HRSDL 0	HRSLR 0	HRSLL 0	Stereo Headphone Amp Status
0x0158	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	TIMER[5:0] 0	1	0	1	0	0	Stereo Headphone Amp Timer
0x0160	R/W	- -	- -	- -	- -	LXDR 0	LXDL 0	LXLR 0	LXLL 0	- -	- -	- -	- -	RXDR 0	RXDL 0	RXLR 0	RXLL 0	Stereo Speaker Amp Input Select
0x0162	R/W	- -	- -	LXV[5:0 0	0	0	0	0	0	- -	- -	0	0	RXV[5:0] 0	0	0	0	Stereo Speaker Amp Volume
0x0164	R/W	- -	- -	- -	- -	- -	- -	- -	LXG 0	- -	- -	- -	- -	- -	- -	- -	RXG 0	Stereo Speaker Amp Gain Control

0x0166	R	- -	- -	- -	- -	LXSDR 0	LXSDL 0	LXSLR 0	LXSLL 0	- -	- -	- -	- -	RXSDR 0	RXSDL 0	RXSLR 0	RXSLL 0	Stereo Speaker Amp Status
Interrupt Control Registers																		
0x0010	R	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	APRB 1	- -	Interrupt Status
0x0012	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	APENB 0	- -	Interrupt Enable
0x0014	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	ISS 0	Interrupt Polarity

Detailed Description of the Registers

Note: "-" indicates a reserved bit. They return "0" for reads. Always write "0" to the bit. If a"1"is written to this bit, the operations cannot be guaranteed.

Clock Select Register(Address 0x0004; Access R/W)

Clock, Reset Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
-	-	-	-	-	-	-	-	-	-	-	PLLSRC[1:0]		CLK256SEL[2:0]		
-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0

The register is used to select source clock input to PLL and select audio clock clk256fs. The register manipulation is prohibited during audio output. It generate noise.

PLLSRC[1:0]

Select source clock of PLL.

PLLSRC[1:0]	Description
00	No clock input.
x1	External clock from SYSCLK pin input.
10	External clock from SAI_LRCLK pin input. Do not set this mode when SAI is in the master mode.

CLK256SEL[2:0]

Select audio clock clk256fs.

CLK256SEL[2:0]	Description **説明**
000	No audio clock clk256fs.
xx1	PLL output clock.
x10	1/2 PLL output clock.
100	External clock from MCLKI pin input.

MCLKO Output Control Register(Address 0x0006; Access R/W)

Clock, Reset Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	MCLKOEN 0

This register controls the output of the MCLKO pin.

MCLKOEN

MCLKOEN	Description
0	Fixed at “L”.
1	Audio clock clk256fs output.

Clock Feedback Resistor Control Register (Address 0x0008; Access R/W)

Clock, Reset Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	RFOFF 0

This register controls the feedback resistor for the clock buffer of the SYSCLK pin.

RFOFF bit
For a full swing clock, set this register to “1” which disables the feedback resistor. The current consumption is reduced.

RFOFF	Description
0	A small amplitude clock input is acceptable.
1	Full swing clock must be inputted.

Audio PLL Times 1 Register (Address 0x000A; Access R/W)

Clock, Reset Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
-	-	-	-	-	-	-	-	PLLNVAL[7:0]							
-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0

This register specifies the PLL output frequency along with Audio PLL Times 2 register and Audio PLL Div register. The value can be set from 0x00 to 0xFF. Do not change this register during PLL operation.

Audio PLL Times 2 Register (Address 0x000C; Access R/W)

Clock, Reset Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
PLLMVAL[15:0]															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register specifies the PLL output frequency along with Audio PLL Times 1 register and Audio PLL Div register. The value can be set from 0x0000 to 0xFFFF. Do not change this register during PLL operation.

Audio PLL Div Register (Address 0x000E; Access R/W)

Clock, Reset Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
-	-	-	-	-	-	-	PLLOEN	PLLDVAL[7:0]							
-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0

This register specifies the PLL output frequency along with Audio PLL Times 1 register and Audio PLL Times 2 register. Also this register controls PLL operation.

PLLOEN bit

This bit is to set enable or disable output of PLL. PLLOEN bit can be set without relation with setting of a PLLEN bit of a Sound Path Control register and PLLTMR of an Audio PLL Timer register.

PLLOEN	
0	PLL disable
1	PLL enable

PLLDVAL [7:0] bit

PLLDVAL is specifies the PLL output frequency along with PLLNVAL and PLLMVAL. The value can be set from 0x00 to 0xFF. Do not change these bits during PLL operation.

Setting PLLOEN bit to “1” after setting the following register.

PLLNVAL[7:0] (Audio PLL Times 1 Register)
PLLMVAL[15:0] (Audio PLL Times 2 Register)
PLLDVAL[7:0] (Audio PLL Div Register)

Audio PLL Timer Register (Address 0x0018; Access R/W)

Clock, Reset Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	- -	- -	- -	- -	PLLTMR[7:0] 0	0	0	0	0	0	0	0

This register specifies PLL wait time that is required for PLL start up. Set this register value to be a PLL wait time approximately 11ms. The wait time is calculated by 1 cycle of SYSCLK(tCLOCK) as following formura.

PLL wait time = tCLOCK * (PLLTMR[7:0] * 1024 + 1023)

ExampleSYSCLK=19.2MHz

PLLTMR[7:0] = (11ms – tCLOCK * 1023) / (tCLOCK * 1024)

≅ 205.3

Therefore,

PLLTMR[7:0] = 206 = 0xCE

Set the PLLTMR before PLLEN bit of Sound Path Control Register is set to “1”.

Software Reset Register (Address 0x0020; Access W)

Clock, Reset Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	SOFTRST

This register is for software reset. All registers are reset by writing SOFTRST bit to “1” or “0”.

Sound Path Control Register (Address 0x0100; Access R/W)

Sound Path Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	SAIREN 0	- -	PLLEN 0	DACEN 0	- -	- -	- -	- -	- -	LIL1EN 0	- -	- -	- -	- -	LIR1EN 0

This register is to start or stop line amplifiers, DAC, PLL, and SAI.

SAIREN

This bit is to set the status of SAI receiving operation.

SAIREN	Description
0	SAI stops.
1	SAI starts.

PLLEN

This bit is to set the status of PLL.
Set this bit after set the PLLTMR bits of Audio PLL Timer Register.
This bit is Enable control bit of PLL. PLLEN bit set PLL to start / stop.
Please set PLLEN after setting PLLTMR of an Audio PLL Timer register in order to wait for stability time of PLL.

PLLEN	Description
0	PLL stops.
1	PLL starts.

DACEN

This bit is to set the status of DAC.

DACEN	Description
0	DAC stops.
1	DAC starts.

LIL1EN

This bit is set the status of left channel line input amplifier 1.

LIL1EN	Description
0	Left channel line input amplifier 1 stops.
1	Left channel line input amplifier 1 starts.

LIR1EN

This bit is to set the status of right channel line input amplifier 1.

LIR1EN	Description
0	Right channel line input amplifier 1 stops.
1	Right channel line input amplifier 1 starts.

Sound Effect Enable Register (Address 0x0102; Access R/W)

Sound Path Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	EQEN 0	TBEN 0	SRSEN 0	WOWXTEN 0

This register is to control Sound effecters including SRS Labs audio enhancement technologies(WOWXT) and equalizer.

WOWXTEN

This bit is to enable or disable SRS Labs technologies.

WOWXTEN	Description
0	Disable SRS technology
1	Enable SRS technology

SRSEN

This bit is to enable or disable 3D surround technologies. This bit is only valid when WOWXTEN bit is set to “1”.

SRSEN	Description
0	Disable 3D surround
1	Enable 3D surround

TBEN

This bit is to enable or disable TruBass. This bit is only valid when WOWXTEN bit is set to “1”.

TBEN	Description
0	Disable TruBass
1	Enable TruBass

EQEN

This bit is to enable or disable equalizer effects.

EQEN	Description
0	Disable qualizer effects.
1	Enable equalizer effects.

Digital Mixer SAI Volume Register (Address 0x01A2; Access R/W)

Sound Path Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
-	DMX_VOLSAI_L[6:0]							-	DMX_VOLSAI_R[6:0]						
-	0	0	0	0	0	0	0	-	0	0	0	0	0	0	0

This register is to set input volume from SAI.

DMX_VOLSAI_L [6:0]

This bit is to set left channel input volume from SAI by 0.5dB step. Please see following table.

DMX_VOLSAI_L[6:0]	Volume	DMX_VOLSAI_L[6:0]	Volume	DMX_VOLSAI_L[6:0]	Volume
0	+6.0dB	20	-4.0dB	40	-14.0dB
1	+5.5dB	21	-4.5dB	41	-14.5dB
2	+5.0dB	22	-5.0dB	42	-15.0dB
3	+4.5dB	23	-5.5dB	43	-15.5dB
4	+4.0dB	24	-6.0dB	44	-16.0dB
5	+3.5dB	25	-6.5dB	45	-16.5dB
6	+3.0dB	26	-7.0dB	46	-17.0dB
7	+2.5dB	27	-7.5dB	47	-17.5dB
8	+2.0dB	28	-8.0dB	48	-18.0dB
9	+1.5dB	29	-8.5dB	49	-18.5dB
10	+1.0dB	30	-9.0dB	50	-19.0dB
11	+0.5dB	31	-9.5dB	51	-19.5dB
12	+0.0dB	32	-10.0dB	52	-20.0dB
13	-0.5dB	33	-10.5dB	53	Mute
14	-1.0dB	34	-11.0dB	54	Mute
15	-1.5dB	35	-11.5dB	•	•
16	-2.0dB	36	-12.0dB	•	•
17	-2.5dB	37	-12.5dB	•	•
18	-3.0dB	38	-13.0dB	126	Mute
19	-3.5dB	39	-13.5dB	127	Mute

DMX_VOLSAI_R [6:0]

This bit is to set right channel input volume from SAI by 0.5dB step. The correspondence of the register value and the volume is the same as DMX_VOLSAI_L [6:0].

Sampling Frequency Setting Register(Address 0x01B6; Access R/W)

Sound Effect Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	0	FRQ[2:0] 1	0

This register is to set the sampling frequency of the 3D surround effect, TruBass and the equalizer effects. When changing the register, please disable the 3D surround effect, TruBass and the equalizer effects.

Register value changing condition

WOWXTEN=EQEN=0 (SRSEN, TBEN: don't care)

SRSEN=TBEN=EQEN=0(WOWXTEN: don't care)

FRQ [2:0]

Set the sampling frequency as same as SAI.

FRQ[2:0]	Description
000	Write prohibited *
001	Write prohibited *
010	16 kHz
011	22.05 kHz
100	24 kHz
101	32 kHz
110	44.1 kHz
111	48 kHz

***** No guarantee of proper operation.

SRS 3D Mode Register (Address 0x01B0; Access R/W)

Sound Effect Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	3DMODE 0

This register specifies 3D surround mode.

3DMODE
This bit is to select 3D surround mode. Please disable the 3D surround effect(SRSEN=0) before change this bit.

3DMODE	Description
0	SRS Headphone
1	SRS3D Extreme mode (For closely spaced speaker)

SRS Headphone Control Register (Address 0x01B2; Access R/W)

Sound Effect Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
-	-	-	-	-	-	-	-	-	SRSHCNT[6:0]						
-	-	-	-	-	-	-	-	-	1	1	0	0	1	1	0

This register controls the effect value of the SRS Headphone.

SRSHCNT [6:0]
The bits are to set the SRS Headphone value. The value can be set from 0x00 to 0x7F.

SRS 3D Extreme Control Register (Address 0x01B4; Access R/W)

Sound Effect Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
-	-	-	-	-	-	-	-	-	SRS3DECNT[6:0]						
-	-	-	-	-	-	-	-	-	1	1	0	0	1	1	0

This register controls the effect value of the SRS 3D Extreme mode.

SRS3DECNT [6:0]
The bits are to set the SRS 3D Extreme mode value. The value can be set from 0x00 to 0x7F.

SRS TruBass Size Register (Address 0x01B8; Access R/W)

Sound Effect Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	- -	- -	- -	- -	-	- -	- -	- -	- -	- -	- -	TBSIZE 0

This register specifies speaker cut off frequency.

TBSIZE bit:
This bit is to select cut off frequency.
Please disable the TruBass effect(TBEN=0) before change this bit.

TBSIZE	TruBass speaker size (cut-off frequency) [Hz]
0	60
1	400

SRS TruBass Control Register (Address 0x01BA; Access R/W)

Sound Effect Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
-	-	-	-	-	-	-	-	-	SRSTBCNT[6:0]						
-	-	-	-	-	-	-	-	-	1	1	0	0	1	1	0

This register controls the effect value of the TruBass.

SRSTBCNT [7:0]
The bits are to set the SRS TruBass value. The value can be set from 0x00 to 0x7F.

EQ Band 0 Gain Setting Register (Address 0x01C2; Access R/W)

Sound Effect Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
-	-	-	-	-	-	-	-	-	-	-	EQGAIN0[4:0]				
-	-	-	-	-	-	-	-	-	-	-	0	1	0	1	0

This register is to set gain of equalizer band 0.

EQGAIN0 [4:0]

The bits to set gain of equalizer band 0. Please see following table.

EQGAIN0[4:0]	Output level	
	dB	Linear
0x00	+10dB	3.1622777
0x01	+9dB	2.8183829
0x02	+8dB	2.5118864
0x03	+7dB	2.2387211
0x04	+6dB	1.9952623
0x05	+5dB	1.7782794
0x06	+4dB	1.5848932
0x07	+3dB	1.4125375
0x08	+2dB	1.2589254
0x09	+1dB	1.1220185
0x0A	0dB	1.0000000
0x0B	-1dB	0.8912509
0x0C	-2dB	0.7943282
0x0D	-3dB	0.7079458
0x0E	-4dB	0.6309573
0x0F	-5dB	0.5623413
0x10	-6dB	0.5011872
0x11	-7dB	0.4466836
0x12	-8dB	0.3981072
0x13	-9dB	0.3548134
0x14	-10dB	0.3162278
0x15 to 0x1F	Prohibited	

Following table shows the relation between band number and frequency.

Sampling Frequency	Band0		Band1		Band2		Band3		Band4		
	cross	center	cross	center	cross	center	cross	center	cross	center	cross
16000Hz	30	-	150	281	527	987	1850	3467	6498	-	7999
22050Hz	30	-	197	369	691	1295	2428	4550	8528	-	11024
24000Hz	30	-	234	439	823	1542	2890	5417	10152	-	11999
32000Hz	30	-	200	400	800	1600	3200	6400	12800	-	15999
44100Hz	30	-	250	500	1000	2000	4000	8000	16000	-	22049
48000Hz	30	-	250	500	1000	2000	4000	8000	16000	-	23999

Center means the center frequency of each band.

EQ Band 1 Gain Setting Register (Address 0x01C4; Access R/W)

Sound Effect Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	EQGAIN1[4:0] 0	1	0	1	0

This register is to set gain of equalizer band 1.

EQGAIN1 [4:0]
The bits to set gain of equalizer band 1. Please see following table.

EQGAIN1[4:0]	Output level	
	dB	Linear
0x00	+10dB	3.1622777
0x01	+9dB	2.8183829
0x02	+8dB	2.5118864
0x03	+7dB	2.2387211
0x04	+6dB	1.9952623
0x05	+5dB	1.7782794
0x06	+4dB	1.5848932
0x07	+3dB	1.4125375
0x08	+2dB	1.2589254
0x09	+1dB	1.1220185
0x0A	0dB	1.0000000
0x0B	-1dB	0.8912509
0x0C	-2dB	0.7943282
0x0D	-3dB	0.7079458
0x0E	-4dB	0.6309573
0x0F	-5dB	0.5623413
0x10	-6dB	0.5011872
0x11	-7dB	0.4466836
0x12	-8dB	0.3981072
0x13	-9dB	0.3548134
0x14	-10dB	0.3162278
0x15 to 0x1F	Prohibited	

EQ Band 2 Gain Setting Register (Address 0x01C6; Access R/W)

Sound Effect Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
-	-	-	-	-	-	-	-	-	-	-	EQGAIN2[4:0]				
-	-	-	-	-	-	-	-	-	-	-	0	1	0	1	0

This register is to set gain of equalizer band 2.

EQGAIN2 [4:0]

The bits to set gain of equalizer band 2. Please see following table.

EQGAIN2[4:0]	Output level	
	dB	Linear
0x00	+10dB	3.1622777
0x01	+9dB	2.8183829
0x02	+8dB	2.5118864
0x03	+7dB	2.2387211
0x04	+6dB	1.9952623
0x05	+5dB	1.7782794
0x06	+4dB	1.5848932
0x07	+3dB	1.4125375
0x08	+2dB	1.2589254
0x09	+1dB	1.1220185
0x0A	0dB	1.0000000
0x0B	-1dB	0.8912509
0x0C	-2dB	0.7943282
0x0D	-3dB	0.7079458
0x0E	-4dB	0.6309573
0x0F	-5dB	0.5623413
0x10	-6dB	0.5011872
0x11	-7dB	0.4466836
0x12	-8dB	0.3981072
0x13	-9dB	0.3548134
0x14	-10dB	0.3162278
0x15 to 0x1F	Prohibited	

EQ Band 3 Gain Setting Register (Address 0x01C8; Access R/W)

Sound Effect Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	EQGAIN3[4:0] 0	1	0	1	0

This register is to set gain of equalizer band 3.

EQGAIN3 [4:0]
The bits to set gain of equalizer band 3. Please see following table.

EQGAIN3[4:0]	Output level	
	dB	Linear
0x00	+10dB	3.1622777
0x01	+9dB	2.8183829
0x02	+8dB	2.5118864
0x03	+7dB	2.2387211
0x04	+6dB	1.9952623
0x05	+5dB	1.7782794
0x06	+4dB	1.5848932
0x07	+3dB	1.4125375
0x08	+2dB	1.2589254
0x09	+1dB	1.1220185
0x0A	0dB	1.0000000
0x0B	-1dB	0.8912509
0x0C	-2dB	0.7943282
0x0D	-3dB	0.7079458
0x0E	-4dB	0.6309573
0x0F	-5dB	0.5623413
0x10	-6dB	0.5011872
0x11	-7dB	0.4466836
0x12	-8dB	0.3981072
0x13	-9dB	0.3548134
0x14	-10dB	0.3162278
0x15 to 0x1F	Prohibited	

EQ Band 4 Gain Setting Register(Address 0x01CA; Access R/W)

Sound Effect Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
-	-	-	-	-	-	-	-	-	-	-	EQGAIN4[4:0]				
-	-	-	-	-	-	-	-	-	-	-	0	1	0	1	0

This register is to set gain of equalizer band 4.

EQGAIN4 [4:0]

The bits to set gain of equalizer band 4. Please see following table.

EQGAIN4[4:0]	Output level	
	dB	Linear
0x00	+10dB	3.1622777
0x01	+9dB	2.8183829
0x02	+8dB	2.5118864
0x03	+7dB	2.2387211
0x04	+6dB	1.9952623
0x05	+5dB	1.7782794
0x06	+4dB	1.5848932
0x07	+3dB	1.4125375
0x08	+2dB	1.2589254
0x09	+1dB	1.1220185
0x0A	0dB	1.0000000
0x0B	-1dB	0.8912509
0x0C	-2dB	0.7943282
0x0D	-3dB	0.7079458
0x0E	-4dB	0.6309573
0x0F	-5dB	0.5623413
0x10	-6dB	0.5011872
0x11	-7dB	0.4466836
0x12	-8dB	0.3981072
0x13	-9dB	0.3548134
0x14	-10dB	0.3162278
0x15 to 0x1F	Prohibited	

SAI Control 1 Register (Address 0x0190; Access R/W)

SAI Interface Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	MSBI 0	ISSCKI 0	AFOI[1:0] 0	0	DLYI 0	WSLI 0	- -	- -	- -	- -	- -	- -

This register controls the setting for the SAI receive format. Do not change this register during operation of the SAI.

WSLI

This bit is to select SAI_LRCLK polarity of ML2611.

WSLI	Description
0	LEFT channel is received when SAI_LRCLK is “L” level.
1	LEFT channel is received when SAI_LRCLK is “H” level.

DLYI

This bit is to specify the one clock delay.

DLYI	Description
0	One clock delay in serial output data from master device.
1	No delay in serial output data from master device.

AFOI [1:0]

These bits are to set left-justify or right-justify. In case of the slave mode, these bits are ignored and fixed at left-justify.

AFOI[1:0]	Description
00	32fs
01	Left-justify.
10	Right-justify.
11	Prohibited.

ISSCKI

This bit is to set 32fs or 64fs. In case of the slave mode, this bit is ignored and fixed at 32fs.

ISSCKI	Description
0	32fs
1	64fs

AFOI, ISSCKI Combination.

AFOI[1:0]	ISSCKI	Operation
00	0	32FS 16bit (Default)
01		32FS 16bit *1
10		32FS 16bit *1
00	1	32FS 16bit *1
01		64FS 16bit Left-justify.
10		64FS 16bit Right-justify.

***1** Same as default setting

MSBI

This bit is to set MSB-first or LSB-first. In case of the slave mode, this bit is ignored and fixed at MSB-first.

MSBO	Description
0	MSB-first.
1	LSB-first.

SAI Control 2 Register (Address 0x0192; Access R/W)

SAI Interface Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	MST 1

This register is to set master mode or slave mode of the SAI. Do not change this register during SAI operation.

MST

This bit is to set master mode or slave mode of the SAI.

MST	Description
0	Master mode.
1	Slave mode.

Stereo Line Input Timer Register (Address 0x0110; Access R/W)

Input/Output Amplifiers Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	LITIMER[4:0] 0	1	1	0

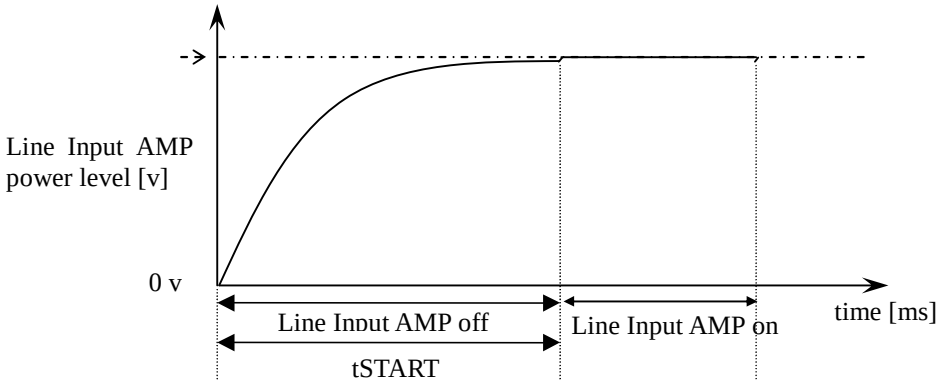
This register is to set the time(tSTART) from enabling the LIL1EN and LIR1EN of the Sound Path Control Register to Analog input operation(Line operation start).
If tSTART is not enough, pop noise may be generated. Please decide tSTART value based on the evaluation since tSTART depends on the input capacitance of LI_LIN1/LI_RIN1 pins. Please refer to the following formula.

tSTART(s) ≅coupling capacitance*30(kΩ)*4

Input coupling capacitance is recommended as 0.22uF. In this case, tSTART becomes over 26ms.
The following table shows the relation between tSTART and Register.

(Analog Clock =2kHz)

TIMER[4:0] bit	tSTART (ms)	TIMER[4:0] bit	tSTART (ms)
0x00	0	0x08	40
0x01	5	0x09	45
0x02	10	0x0A	50
0x03	15	0x0B	55
0x04	20	0x0C	60
0x05	25	0x0D	65
0x06	30	0x0E	70
0x07	35	0x0F	75



tSTART＞26ms (Input coupling capacitance＝0.22uF)

Analog Input Clock Setting Register (Address 0x0112; Access R/W)

Input/Output Amplifiers Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
-	PC[6:0]							-	-	-	-	ADIV[3:0]			
-	0	0	0	0	0	0	0	-	-	-	-	0	0	0	0

This register is to set the internal analog control clock generation.. Adjust this register value to approximatery 2kHz (0.5ms) internal clock is generated.

Analog control clock frequency = (fCLOCK / (PC+1)) / 2^ADIV

fCLOCK: Input clock frequency for SYSCLK pin
PC: PC[6:0] value
ADIV: ADIV[3:0] value

(Example)
fCLOCK=19.2MHz

(PC+1) *2^ADIV = 19200[kHz] / 2[kHz]
(PC+1) *2 ^ ADIV = 9600 = 75 * 128
PC = 74
ADIV = 7

PC[6:0]	(PC+1)
0	1
1	2
. .	. .
126	127
127	128

ADIV[3:0]	2^ADIV	ADIV[3:0]	2^ADIV
0	1	6	64
1	2	7	128
2	4	8	256
3	8	9	512
4	16	10-15	Prohibited
5	32		

Stereo Line Input Ch1 Volume Register (Address 0x0114; Access R/W)

Input/Output Amplifiers Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
-	-	LIV1[5:0]						-	-	RIV1[5:0]					
-	-	0	0	0	0	0	0	-	-	0	0	0	0	0	0

This register is to set the volume of the stereo line input amplifier.

LIV1 [5:0]
These bits are to set the left 1 channel volume of the stereo line input amplifier. Please see following table.

LIV1 [5:0]	Volume [dB]	LIV1 [5:0]	Volume [dB]	LIV1 [5:0]	Volume [dB]
0x00	6	0x10	-2	0x20	-14
0x01	5.5	0x11	-2.5	0x21	-15
0x02	5	0x12	-3	0x22	-16
0x03	4.5	0x13	-3.5	0x23	-17
0x04	4	0x14	-4	0x24	-18
0x05	3.5	0x15	-4.5	0x25	-19
0x06	3	0x16	-5	0x26	-20
0x07	2.5	0x17	-5.5	0x27	-22
0x08	2	0x18	-6	0x28	-24
0x09	1.5	0x19	-7	0x29	-26
0x0A	1	0x1A	-8	0x2A	-28
0x0B	0.5	0x1B	-9	0x2B	Prohibited
0x0C	0	0x1C	-10	•	•
0x0D	-0.5	0x1D	-11	•	•
0x0E	-1	0x1E	-12	•	•
0x0F	-1.5	0x1F	-13	0x3F	Prohibited

RIV1 [5:0]
These bits are to set the right 1 channel volume of the stereo line input amplifier. The correspondence of the register value and the volume is the same as LIV1[5:0].

Stereo Line Input Status Register (Address 0x011E; Access R)

Input/Output Amplifiers Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	- -	- -	- -	LST0 0	- -	- -	- -	- -	- -	- -	- -	RST0 0

This register is to show status of each stereo line input. The relation between these bits and each input pin is as follows.

Bit	Description	Bit	Description
LST0	Status of the LI_LIN1 pin.	RST0	Status of the LI_RIN1 pin.

The relation between bit value and status is as follow.

LST0, RST0	Description
0	The stereo line input cannot be used.
1	The stereo line input can be used.

Stereo Headphone Amp Input Select Register (Address 0x0150; Access R/W)

Input/Output Amplifiers Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	HLDR 0	HLDL 0	HLLR 0	HLLL 0	- -	- -	- -	- -	HRDR 0	HRDL 0	HRLR 0	HRLL 0

This register is to select input signal to the stereo headphone amplifiers. The relation between each bit and analog input is as follow.

Bit	Description
HLDR	Enable/disable selection of the DAC right channel input to the left channel stereo headphone amplifiers.
HLDL	Enable/disable selection of the DAC left channel input to the left channel stereo headphone amplifiers.
HLLR	Enable/disable selection of the right channel line input to the left channel stereo headphone amplifiers.
HLLL	Enable/disable selection of the left channel line input to the left channel stereo headphone amplifiers.
HRDR	Enable/disable selection of the DAC right channel input to the right channel stereo headphone amplifiers.
HRDL	Enable/disable selection of the DAC left channel input to the right channel stereo headphone amplifiers.
HRLR	Enable/disable selection of the right channel line input to the right channel stereo headphone amplifiers.
HRLL	Enable/disable selection of the left channel line input to the right channel stereo headphone amplifiers.

The relation between bit value and status is as follow.

Bit	Description
0	Analog input is disabling.
1	Analog input is enabling.

Stereo Headphone Amp Volume Register (Address 0x0152; Access R/W)

Input/Output Amplifiers Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
-	-	HLV[5:0]						-	-	HRV[5:0]					
-	-	0	0	0	0	0	0	-	-	0	0	0	0	0	0

This register is to set the volume of the stereo headphone amplifiers.

HLV [5:0]
This bit is to set the left channel volume of the stereo headphone amplifiers. Please see following table.

HLV[5:0]	Volume [dB]	HLV[5:0]	Volume [dB]	HLV[5:0]	Volume [dB]
0x00	6	0x12	-3	0x24	-18
0x01	5.5	0x13	-3.5	0x25	-19
0x02	5	0x14	-4	0x26	-20
0x03	4.5	0x15	-4.5	0x27	-22
0x04	4	0x16	-5	0x28	-24
0x05	3.5	0x17	-5.5	0x29	-26
0x06	3	0x18	-6	0x2A	-28
0x07	2.5	0x19	-7	0x2B	-30
0x08	2	0x1A	-8	0x2C	-32
0x09	1.5	0x1B	-9	0x2D	-34
0x0A	1	0x1C	-10	0x2E	-36
0x0B	0.5	0x1D	-11	0x2F	-38
0x0C	0	0x1E	-12	0x30	-40
0x0D	-0.5	0x1F	-13	0x31	Mute
0x0E	-1	0x20	-14	•	•
0x0F	-1.5	0x21	-15	•	•
0x10	-2	0x22	-16	•	•
0x11	-2.5	0x23	-17	0x3F	Mute

HRV [5:0]
This bit is to set the right channel volume of the stereo headphone amplifiers. The correspondence of the register value and the volume is the same as HLV[5:0].

Stereo Headphone Amp Gain Control Register (Address 0x0154; Access R/W)

Input/Output Amplifiers Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	- -	- -	- -	HLG 0	- -	- -	- -	- -	- -	- -	- -	HRG 0

This register is to control the stereo headphone amplifiers gain.

HLG

This bit specifies the left channel headphone amplifiers gain.The following table shows the reration between Stereo Headphone Amp Input Select Register,HLG andStereo Headphone Amp Gain.

Headphone Amp Input selector				Headphone Amp Gain Control	
HLLL	HLLR	HLDL	HLDR	HLG=0	HLG=1
0	0	0	0	Not active	Same as left
0	0	0	1	HLDR	Same as left
0	0	1	0	HLDL	Same as left
0	0	1	1	(HLDL+HLDR)/2	HLDL+HLDR
0	1	0	0	HLLR	Same as left
0	1	0	1	HLLR+HLDR	Same as left
0	1	1	0	HLLR+HLDL	Same as left
0	1	1	1	HLLR+(HLDL+HLDR)/2	HLLR+HLDL+HLDR
1	0	0	0	HLLL	Same as left
1	0	0	1	HLLL+HLDR	Same as left
1	0	1	0	HLLL+HLDL	Same as left
1	0	1	1	HLLL+(HLDL+HLDR)/2	HLLL+HLDL+HLDR
1	1	0	0	(HLLL+HLLR)/2	HLLL+HLLR
1	1	0	1	(HLLL+HLLR)/2+HLDR	HLLL+HLLR+HLDR
1	1	1	0	(HLLL+HLLR)/2+HLDL	HLLL+HLLR+HLDL
1	1	1	1	(HLLL+HLLR)/2+(HLDR+HLDL)/2	HLLL+HLLR+HLDL+HLDR

HRG

This bit specifies the right channel headphone amplifiers gain.The correspondence of the Headphone Amp Input selector and the Headphone Amp Gain is the same as left channel.

Notice:

When the register is changed, please set disenabling “Stereo Headphone Amp Input Select” register. When “Stereo Headphone Amp Input Select” is changed from disenabling to enabling, the register value is applied.

Stereo Headphone Amp Status Register (Address 0x0156; Access R)

Input/Output Amplifiers Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	HLSDR 0	HLSDL 0	HLSLR 0	HLSLL 0	- -	- -	- -	- -	HRSDR 0	HRSDL 0	HRSLR 0	HRSLL 0

This register is to show status of the stereo headphone amplifiers. The relation between each bit and analog input is as follow.

Bit	Description
HLSDR	Status of the DAC right channel input to left channel stereo headphone amplifiers.
HLSDL	Status of the DAC left channel input to left channel stereo headphone amplifiers.
HLSLR	Status of the right channel line input to left channel stereo headphone amplifiers.
HLSLL	Status of the left channel line input to left channel stereo headphone amplifiers.
HRSDR	Status of the DAC right channel input to right channel stereo headphone amplifiers.
HRSDL	Status of the DAC left channel input to right channel stereo headphone amplifiers.
HRSLR	Status of the right channel line input to right channel stereo headphone amplifiers.
HRSLL	Status of the left channel line input to right channel stereo headphone amplifiers.

The relation between bit value and status is as follow.

Bit	Description
0	Analog input is not active.
1	Analog input is active.

Stereo Headphone Amp Timer Register (Address 0x0158; Access R/W)

Input/Output Amplifiers Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	TIMER[5:0] 0	1	0	1	0	0

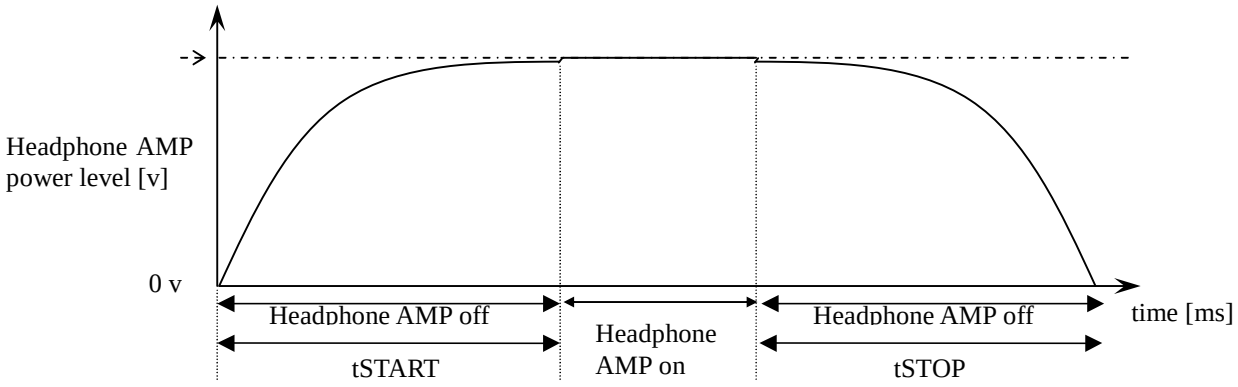
This register is to specify the time(tSTART/tSTOP) from the Stereo Headphone Amp Input Select Register setting change to Stereo Headphone Amp Ststus register change(change the Headphone Amp operating status).
If tSTART/tSTOP is not enough, pop noise may be generated. Please decide tSTART/tSTOP value based on the evaluation.
Please refer to the following formula.

tSTART/tSTOP(s) ≅HP_CAP capacitance*100(kΩ)*5

HP_CAP capacitance is recommended as 1uF. In this case, tSTART/tSTOP becomes over 500ms.
The following table shows the relation between tSTART/tSTOP and Register.

(Analog Clock =2kHz)

TIMER[5:0] bit	tSTART/tSTOP (ms)	TIMER[5:0] bit	tSTART/tSTOP (ms)
0x00	0	0x10	400
0x01	25	0x11	425
0x02	50	0x12	450
0x03	75	0x13	475
0x04	100	0x14	500
0x05	125	'	'
0x06	150	'	'
0x07	175	'	'
0x08	200	0x38	1400
0x09	225	0x39	1425
0x0A	250	0x3A	1450
0x0B	275	0x3B	1475
0x0C	300	0x3C	1500
0x0D	325	0x3D	1525
0x0E	350	0x3E	1550
0x0F	375	0x3F	1575



tSTART/tSTOP＞500ms (HP_CAP＝1uF)

Stereo Speaker Amp Input Select Register(Address 0x0160; Access R/W)

Input/Output Amplifiers Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	LXDR 0	LXDL 0	LXLR 0	LXLL 0	- -	- -	- -	- -	RXDR 0	RXDL 0	RXLR 0	RXLL 0

This register is to select input signal to the stereo speaker amplifier. The relation between each bit and analog input is as follow.

Bit	Description
LXDR	Enable/disable selection of the DAC right channel input for the streo speaker amplifier left channel.
LXDL	Enable/disable selection of the DAC left channel input for the streo speaker amplifier left channel.
LXLR	Enable/disable selection of the right channel line input for the streo speaker amplifier left channel.
LXLL	Enable/disable selection of the left channel line input for the streo speaker amplifier left channel.
RXDR	Enable/disable selection of the DAC right channel input for the streo speaker amplifier right channel.
RXDL	Enable/disable selection of the DAC left channel input for the streo speaker amplifier right channel.
RXLR	Enable/disable selection of the right channel line input for the streo speaker amplifier right channel.
RXLL	Enable/disable selection of the left channel line input for the streo speaker amplifier right channel.

The relation between bit value and status is as follow.

Bit	Description
0	Analog input is disabling.
1	Analog input is enabling.

Stereo Speaker Amp Volume Register(Address 0x0162; Access R/W)

Input/Output Amplifiers Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
-	-	LXV[5:0]						-	-	RXV[5:0]					
-	-	0	0	0	0	0	0	-	-	0	0	0	0	0	0

This register is to set the volume of the stereo speaker amplifier.

RXV [5:0]
These bits are to set the volume of the stereo speaker amplifier right channel. The following table shows volume level of SP_ROUT+ pin. If speaker is connected as BTL, volume level is added +6dB.

RXV[5:0]	Volume [dB]	RXV[5:0]	Volume [dB]	RXV[5:0]	Volume [dB]
0x00	12	0x12	3	0x24	-12
0x01	11.5	0x13	2.5	0x25	-13
0x02	11	0x14	2	0x26	-14
0x03	10.5	0x15	1.5	0x27	-16
0x04	10	0x16	1	0x28	-18
0x05	9.5	0x17	0.5	0x29	-20
0x06	9	0x18	0	0x2A	-22
0x07	8.5	0x19	-1	0x2B	-24
0x08	8	0x1A	-2	0x2C	-26
0x09	7.5	0x1B	-3	0x2D	-28
0x0A	7	0x1C	-4	0x2E	-30
0x0B	6.5	0x1D	-5	0x2F	-32
0x0C	6	0x1E	-6	0x30	-34
0x0D	5.5	0x1F	-7	0x31	Mute
0x0E	5	0x20	-8	•	•
0x0F	4.5	0x21	-9	•	•
0x10	4	0x22	-10	•	•
0x11	3.5	0x23	-11	0x3F	Mute

LXV [5:0]
These bits are to set the volume of the stereo speaker amplifier left channel.The correspondence of the register value and the volume is the same as RXV[5:0].

Stereo Speaker Amp Gain Control Register(Address 0x0164; Access R/W)

Input/Output Amplifiers Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	- -	- -	- -	LXG 0	- -	- -	- -	- -	- -	- -	- -	RXG 0

This register is to control the stereo speaker amplifiers gain.

RXG

This bit specifies the right channel stereo speaker amplifiers gain.The following table shows the reration between Stereo Speaker Amp Input Select Register,RXG andStereo Speaker Amp Gain.

Stereo Speaker Amp Input Select Register				Stereo Speaker Amp Gain	
RXLL	RXLR	RXDL	RXDR	RXG=0	RXG=1
0	0	0	0	Not active	Same as left
0	0	0	1	RXDR	Same as left
0	0	1	0	RXDL	Same as left
0	0	1	1	(RXDL+RXDR)/2	RXDL+RXDR
0	1	0	0	RXLR	Same as left
0	1	0	1	RXLR+RXDR	Same as left
0	1	1	0	RXLR+RXDL	Same as left
0	1	1	1	RXLR+(RXDL+RXDR)/2	RXLR+RXDL+RXDR
1	0	0	0	RXLL	Same as left
1	0	0	1	RXLL+RXDR	Same as left
1	0	1	0	RXLL+RXDL	Same as left
1	0	1	1	RXLL+(RXDL+RXDR)/2	RXLL+RXDL+RXDR
1	1	0	0	(RXLL+RXLR)/2	RXLL+RXLR
1	1	0	1	(RXLL+RXLR)/2+RXDR	RXLL+RXLR+RXDR
1	1	1	0	(RXLL+RXLR)/2+RXDL	RXLL+RXLR+RXDL
1	1	1	1	(RXLL+RXLR)/2+(RXDR+RXDL)/2	RXLL+RXLR+RXDL+RXDR

LXG

This bit specifies the left channel stereo speaker amplifiers gain.。The correspondence of the Stereo Speaker Amp Input selector and the Stereo Speaker Amp Gain is the same as left channel.

Notice:

When the register is changed, please set disenabling “Stereo Speaker Amp Input Select” register. When “Stereo Speaker Amp Input Select” is changed from disenabling to enabling, the register value is applied.

Stereo Speaker Amp Status Register (Address 0x0166; Access R)

Input/Output Amplifiers Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	LXSDR 0	LXSDL 0	LXSLR 0	LXSLL 0	- -	- -	- -	- -	RXSDR 0	RXSDL 0	RXSLR 0	RXSLL 0

This register is to show status of the stereo speaker amplifier. The relation between each bit and analog input is as follow.

Bit	Description
LXSDR	Status of the DAC right channel input for the left channel stereo speaker amplifire.
LXSDL	Status of the DAC left channel input for the left channel stereo speaker amplifire.
LXSLR	Status of the right channel line input for the left channel stereo speaker amplifire.
LXSLL	Status of the left channel line input for the left channel stereo speaker amplifire.
RXSDR	Status of the DAC right channel input for the right channel stereo speaker amplifire.
RXSDL	Status of the DAC left channel input for the right channel stereo speaker amplifire.
RXSLR	Status of the right channel line input for the right channel stereo speaker amplifire.
RXSLL	Status of the left channel line input for the right channel stereo speaker amplifire.

The relation between bit value and status is as follow.

Bit	Description
0	Analog input is not active.
1	Analog input is active.

Interrupt Status Register (Address 0x0010; Access R)

Interrupt Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	APRB 1	- -

The interrupt ststus can be confirmed by reading this register. APRB interrupt signal (IRQ output) can be cleared by reading this register. However the value of this register will not change. This register is active when the interrupt is disabled by Interrupt Enable register.

APRB

After the AMP and PLL operation are set (enabled/disabled), this bit is set to "1" when actual AMP and/or PLL operation become the same status as the register setting. When actual AMP and PLL operation become the deferent status, this bit is clear to "0".

APRB	Description
0	deferent status
1	same status

This bit is indicated as the result of comparison between 19 operation settings and actual operation ststus.

Interrupt Source	Register Bit	Interrupt Source	Register Bit
PLL operation enable	Sound Path Control PLLEN		
Stereo Line Input Ch1,Left Select	Sound Path Control LIL1EN	Stereo Line Input Ch1,Right Select	Sound Path Control LIR1EN
HeadphoneAMP Right Input DAC-R Select	Stereo Headphone Amp Input Select HRDR	SpeakerAMP Right Input DAC-R Select	Speaker Amp Input Select RXDR
HeadphoneAMP Right Input DAC-L Select	Stereo Headphone Amp Input Select HRDL	SpeakerAMP Right Input DAC-L Select	Speaker Amp Input Select RXDL
HeadphoneAMP Right Input LINEIN-R Select	Stereo Headphone Amp Input Select HRLR	SpeakerAMP Right Input LINEIN-R Select	Speaker Amp Input Select RXLR
HeadphoneAMP Right Input LINEIN-L Select	Stereo Headphone Amp Input Select HRLL	SpeakerAMP Right Input LINEIN-L Select	Speaker Amp Input Select RXLL
HeadphoneAMP Left Input DAC-R Select	Stereo Headphone Amp Input Select HLDR	SpeakerAMP Left Input DAC-R Select	Speaker Amp Input Select LXDR
HeadphoneAMP Left Input DAC-L Select	Stereo Headphone Amp Input Select HLDL	SpeakerAMP Left Input DAC-L Select	Speaker Amp Input Select LXDL
HeadphoneAMP Left Input LINEIN-R Select	Stereo Headphone Amp Input Select HLLR	SpeakerAMP Left Input LINEIN-R Select	Speaker Amp Input Select LXLR
HeadphoneAMP Left Input LINEIN-L Select	Stereo Headphone Amp Input Select HLLL	SpeakerAMP Left Input LINEIN-L Select	Speaker Amp Input Select LXLL

Interrupt Enable Register (Address 0x0012; Access R/W)

Interrupt Control Register															
b15	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
(Initial)															
-	-	-	-	-	-	-	-	-	-	-	-	-	-	APENB	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-

This register is to set interrupt enable. Interrupt Porality Register must be set before this register is enabled.

APENB
This bit is to set interrupt enable/disable

APENB	Description
0	Interrupt disable
1	Interrupt enable

Interrupt Polarity Register (Address 0x0014; Access R/W)

Interrupt Control Register															
b15 (Initial)	b14	b13	b12	b11	b10	b09	b08	b07	b06	b05	b04	b03	b02	b01	b00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	ISS 0

This register is to set polarity of interrupt status of IRQ pin.

ISS	Descriptiom
0	Nomal polarity (interrupt:IRQ＝H)
1	Polarity reveresed (interrupt:IRQ＝L)

Revision History

Date	Page	Notes	Revision
06/06/27	All	Release preliminaly version 0.0.0	0.0.01
06/07/19	All	Release preliminaly version 0.1.1	0.1.1
06/07/26	17	Clock control function block diagram	0.1.2
06/08/22	5	Insert LINEAMP, HPAMP and DACAMP in the Block Diagram	0.1.3
	7	Correct the Power of the SYSCLK Power in the Pin Description	
	9	Delete the Condition of the MCLK Supply Voltage in the Recommended Operation Condition	
	10	Correct the Condition of IIH and IIL in the DC Characteristics	
	10	Add the Condition of IDDO2 in the DC Characteristics	
	11	Change the Min. value of tCH and tCL in the AC Characteristics	
	16, 28, 36	Delete PLLOEN	
06/08/31	4, 5, 16, 29, 55, 56	Delete Auto fader function	0.1.4
06/09/04	30, 56	Add Streo Line Input Timer	0.1.5
	30, 64	Cahnge Streo Headphone Amp Timer Initial value	
06/09/07	4	Change WCSP package size	0.1.6
	5	Delete Auto fader block	
06/09/14	7	Add Pin Layout	0.2.0
	8, 9	Change all Pin No.	
	10	Add Absolute Maximum Ratings parametersAdd Recommended Operating Condition	
07/01/12	8	Change value of capacitor connected to SPLVDD, SPRVDD, DACVDD, AVDD	0.3.0
	8	Connect HP_CAP and BIAS to DACGND instead of AGND	
	8	Add type of power to HP_CAP, BIAS, LI_LINI, LI_RINI pin	
	8	Add value of parts into circuit of PLLC pin	
	18	Add Power Derating Curves	
	11	Add no-load and no signal into DC Characteristics conditions	
	17	Add Line in input resistance	
	13, 15	Add CL=30pF to condition	
	14, 15	Add direction into pin when SAI operating	
	31, 39	Add PLLOEN bit	
	20	Change the function description of clock	
	29	Change the function description of input/output amp	
07/01/15	20, 59	Correct the calculating formula of analog clock	0.3.1
07/01/23	20, 59	Correct the calculating formula of analog clock	0.3.2
	39	Change description of PLLOEN bit	
	42	Change description of PLLEN bit	
07/02/16	10	Change value of Power Dissipation from 750mW to 1600mW	0.3.3
	8, 21	Change value of capacitor and register on PLLC pin.	
07/02/23	11	Describe specification of IDDS,IDDO	0.3.3
	21	Correct resistor and capacitor size on PLLC pin.	
	21,22	Correct value of PLL related register.	
	21,38,39,40	Correct calcuration for PLL related register.	

	65,70	Add notice of “Stereo Headphone Amp Gain Control” register, and “Stereo Speaker Amp Gain Control” register.	
07/02/28	All	Delete “CONFIDENTIAL”	0.3.4
	8	Add TopView of WCSP package	
	61	Change table of ADIV	
	17	Change Power Supply Sequence	

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