ML2602 DATASHEET

(DIGEST)
Version 1.0.0
Revised on 21-Jun-07

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Contents

General Description

The ML2602 is a high quality 3D surround enhancement LSI for audio applications. The LSI supports two modes, SRS Headphone and SRS3D Extreme, with emphasis on low power through a complete hardwired solution. The ML2602 also incorporates stereo headphone speaker amplifiers, BTL receiver amplifiers, stereo line amplifiers, a mono line amplifier, and 7kΩ stereo amplifiers. Typical applications are mobile phones and portable audio players.

Features

1) CPU I/F
   I2C slave mode
   - 7bit addressing, address 3bit is changeable by pin
   - Support Standard / Fast mode

2) Serial Audio Interface (SAI)
   - Sampling frequency: 16k ,22.05k, 24k, 32k, 44.1k, 48k Hz
   - Channel data length: 16bit
   - LRCLK positive/negative selectable
   - 1bit delay/Left Justified selectable
   - Slave mode
     MSB first
     BCLK 32clock~128clock
   - Master mode
     32fs/64fs selectable
     MSB first/LSB first selectable

3) Sound Effect
   - 3D surround powered by SRS Labs
     SRS headphone: Repositions sound from inside the head to outside the ears
     SRS3D: 3D stereo enhancement from stereo source
   - 5band Equalizer

4) Analog Input
   - Stereo 5 channels
   - Auto fader (pop noise reduction)

5) DAC/ADC
   - 16bit ΔΣ Audio CODEC

6) Output Amplifiers
   - Stereo headphone amplifiers
   - BTL receiver amplifiers
   - Stereo line amplifiers
   - Mono line amplifier
   - 7kΩ stereo amplifiers

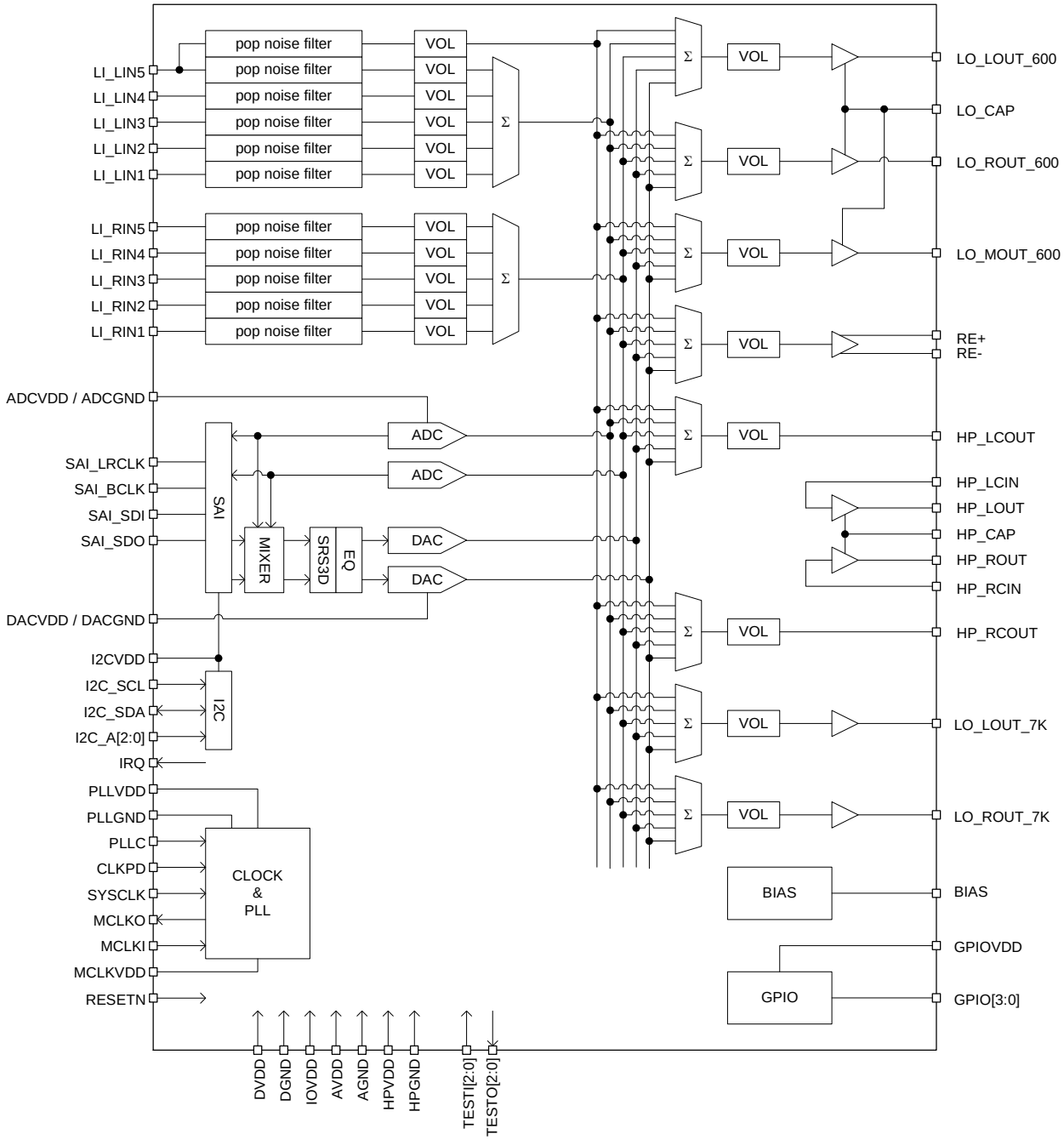
7) GPIO
   - 4bit GPIO

8) Clock
   - 8~20MHz
   - Digital signal or 0.4Vpp sine wave

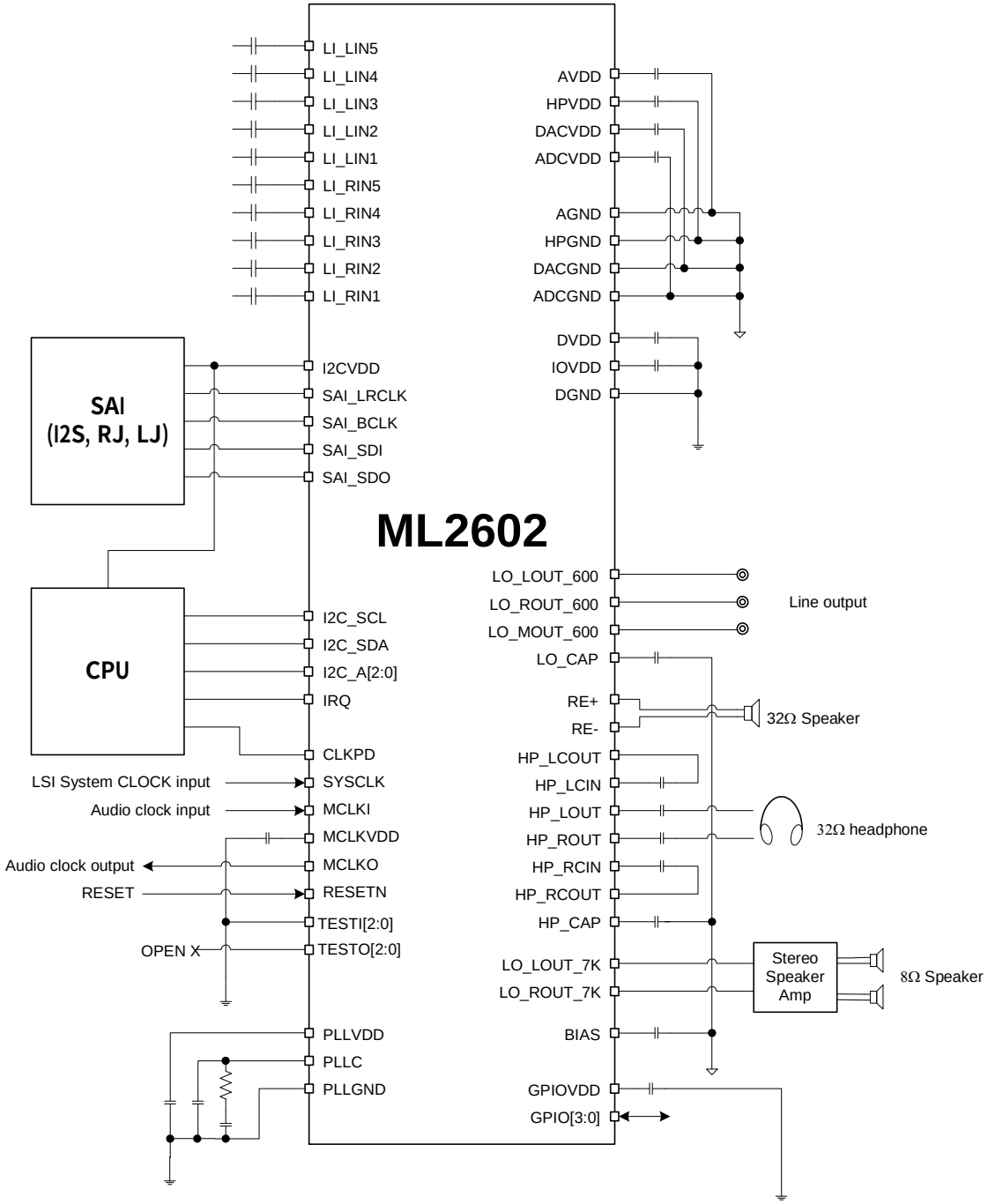
- 256fs

9) Package
Package size: 5.0mm×5.0mm
0.5mm pitch 74pin W-CSP

Block Diagram



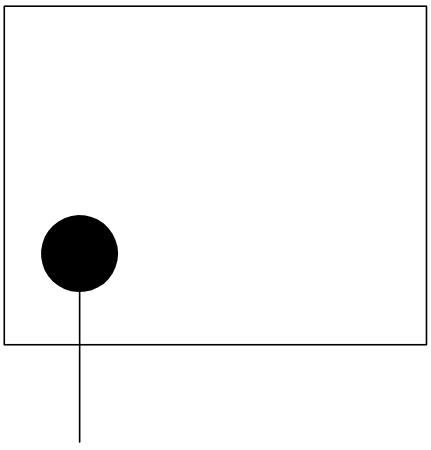
Application Example



Pin Layout

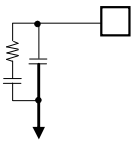
	1	2	3	4	5	6	7	8	9
J	NC	GPIO VDD	GPIO0	DGND	SAI_BCLK	SAI_SDI	I2CVDD	I2C_A2	NC
H	ADCVDD	BIAS	IOVDD	DVDD	SAI_LRCLK	I2C_A0	I2C_SDA	I2C_SCL	RESETN
G	AGND	ADCGND	GPIO1	TESTI4	SAI_ SDO	I2C_A1	CLKPD	TESTI2	TESTO
F	AVDD	GPIO3	GPIO2	TESTI3			TESTI1	TESTI0	MCLK VDD
E	LO_ CAP	LO_ MOUT_ 600	LO_ LOUT 600	LO_ LOUT 7K			MCLKO	MCLKI	DVDD
D	HP_ LCIN	HP_ LCOUT	LO_ ROUT 600	LO_ ROUT 7K				SYSCLK	DGND
C	HP_ RCIN	HP_ RCOUT	HP_ CAP	LI_ RIN1	LI_ LIN3	LI_ LIN5	IRQ	PLLVDD	PLLC
B	HP_ LOUT	HP_ ROUT	RE+	LI_ LIN1	LI_ RIN2	LI_ LIN4	LI_ RIN5	DACGND	PLLGND
A	NC	RE-	HPVDD	HPGND	LI_ LIN2	LI_ RIN3	LI_ RIN4	DACVDD	NC

Bottom View



Top View

Pin Description

Pin No.	Pin Name	I/O	Power	Description
A2	RE-	O	-	Receiver – output.
A3	HPVDD	P	-	Power supply pin for headphone.Please connect 0.1µF capacitor between this pin and HPGND.
A4	HPGND	P	-	Ground pin for headphone.
A5	LI_LIN2	I	-	Left channel line input 2.
A6	LI_RIN3	I	-	Right channel line input 3.
A7	LI_RIN4	I	-	Right channel line input 4.
A8	DACVDD	P	-	Power supply pin for DAC.Please connect 0.1µF capacitor between this pin and DACGND.
B1	HP_LOUT	O	-	Headphone output Left.
B2	HP_ROUT	O	-	Headphone output Right.
B3	RE+	O	-	Receiver + output.
B4	LI_LIN1	I	-	Left channel line input 1.
B5	LI_RIN2	I	-	Right channel line input 2.
B6	LI_LIN4	I	-	Left channel line input 4.
B7	LI_RIN5	I	-	Right channel line input 5.
B8	DACGND	P	-	Ground pin for DAC.
B9	PLLGND	P	-	Ground pin for PLL.
C1	HP_RCIN	I	-	Please connect 47000pF capacitor between this pin and HP_RCOUT.
C2	HP_RCOUT	O	-	Please connect 47000pF capacitor between this pin and HP_RCIN.
C3	HP_CAP	I	-	
C4	LI_RIN1	I	-	Right channel line input 1.
C5	LI_LIN3	I	-	Left channel line input 3.
C6	LI_LIN5	I	-	Left channel line input 5.
C7	IRQ	O	I2CVDD	Interrupt output pin. It outputs “H” level, when interrupt request generated.
C8	PLLVDD	P	-	Power supply pin for PLL.Please connect 0.1µF capacitor between this pin and PLLGND.
C9	PLLC	O	DVDD	Capacitor and resistor connect pin for PLL stable operation. Please set following circuit near by pins as possible. 
D1	HP_LCIN	I	-	Please connect 47000pF capacitor between this pin and HP_LCOUT.
D2	HP_LCOUT	O	-	Please connect 47000pF capacitor between this pin and HP_LCIN.
D3	LO_ROUT600	O	-	Right channel line output.
D4	LO_ROUT7k	O	-	Right channel line output for 7kΩ speaker.
D8	SYSCLK	I	IOVDD	System clock input (8~20MHz).
D9, J4	DGND	P	-	Ground pin for digital.
E1	LO_CAP	I	-	
E2	LO_MOUT600	O	-	Monaural line output.
E3	LO_LOUT600	O	-	Lest channel line output.
E4	LO_LOUT7k	O	-	Left channel line output for 7kΩ speaker.
E7	MCLKO	O	MCLKVDD	Audio clock (256fs) output.
E8	MCLKI	I	MCLKVDD	Audio clock (256fs) input.
E9, H4	DVDD	P	-	Power supply pin for digital.Please connect 0.1µF capacitor between this pin and DGND.
F1	AVDD	P	-	Power supply pin for analog. Please connect 0.1µF capacitor between this pin and AGND.
F2	GPIO3	I/O	GPIOVDD	GPIO input/output 3.
F3	GPIO2	I/O	GPIOVDD	GPIO input/output 2.

F4	TESTI1	I	I2CVDD	Test pin. Please connect it to GND.
F7	TESTO1	O	I2CVDD	Test pin. Please keep it OPEN.
F8	TESTO0	O	I2CVDD	Test pin. Please keep it OPEN.
F9	MCLKVDD	P	-	Power supply pin for MCLK. Please connect 0.1µF capacitor between this pin and DGND.
G1	AGND	P	-	Ground pin for analog.
G2	ADCGND	I	-	Ground pin for ADC.
G3	GPIO1	I/O	GPIOVDD	GPIO input/output 1.
G4	TESTI2	I	I2CVDD	Test pin. Please connect it to GND.
G5	SAI_SDO	O	I2CVDD	Serial data output for SAI.
G6	I2C_A1	I	I2CVDD	Set I2C slave address.
G7	CLKPD	I	I2CVDD	Clock buffer disable control. H: Power down.
G8	TESTO2	O	I2CVDD	Test pin. Please keep it OPEN.
G9	TESTI0	I	I2CVDD	Test pin. Please connect it to GND.
H1	ADCVDD	I	-	Power supply pin for ADC. Please connect 0.1µF capacitor between this pin and ADCGND.
H2	BIAS	I	-	Capacitor connect pin for analog reference voltage. Please connect 1.0µF capacitor between this pin and GND.
H3	IOVDD	P	-	Power supply pin for I/O. Please connect 0.1µF capacitor between this pin and DGND.
H5	SAI_LRCLK	I/O	I2CVDD	LR clock input/output for SAI.
H6	I2C_A0	I	I2CVDD	Set I2C slave address.
H7	I2C_SDA	I/O	IOVDD	I2C bus data input/output.
H8	I2C_SCL	I/O	IOVDD	I2C bus clock input/output.
H9	RESETN	I	I2CVDD	LSI reset input.
J2	GPIOVDD	P	-	Power supply pin for GPIO. Please connect 0.1µF capacitor between this pin and DGND.
J3	GPIO0	I/O	GPIOVDD	GPIO input/output 0.
J5	SAI_BCLK	I/O	I2CVDD	Bit clock input for SAI.
J6	SAI_SDI	I	I2CVDD	Serial data input for SAI.
J7	I2CVDD	P	-	Power supply pin for I2C. Please connect 0.1µF capacitor between this pin and DGND.
J8	I2C_A2	I	I2CVDD	Set I2C slave address.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Core Supply Voltage	DVDD	—	-0.3~3.5	V
DAC Supply Voltage	DACVDD	—	-0.3~3.5	V
ADC Supply Voltage	ADCVDD	—	-0.3~3.5	V
PLL Supply Voltage	PLLVDD	—	-0.3~3.5	V
Headphone Supply Voltage	HPVDD	—	-0.3~4.5	V
Analog Supply Voltage	AVDD	—	-0.3~4.5	V
IO Supply Voltage	IOVDD	—	-0.3~4.5	V
I2C Supply Voltage	I2CVDD	—	-0.3~4.5	V
MCLK Supply Voltage	MCLKVDD	—	-0.3~4.5	V
GPIO Supply Voltage	GPIOVDD	—	-0.3~4.5	V
Input Voltage	Vin	—	-0.3～VDD+0.3	V
Storage Temperature	Tstg	—	-55～+125	°C
Power Dissipation	Pd	Ta=25°C	805	mW

Note) Do not short the output pin to another output pin, power supply pin or GND pin.
(Output pin includes an I/O pin which is in output mode)

Recommended Operating Condition

Parameter	Symbol	Condition	Rating	Unit
Core Supply Voltage	DVDD	DVDD<IOVDD	2.25~2.5	V
DAC Supply Voltage	DACVDD	—	2.25~2.5	V
ADC Supply Voltage	ADCVDD	—	2.25~2.5	V
PLL Supply Voltage	PLLVDD	PLLVDD<IOVDD	2.25~2.5	V
Headphone Supply Voltage	HPVDD	—	2.7~3.6	V
Analog Supply Voltage	AVDD	—	2.7~3.6	V
IO Supply Voltage	IOVDD	—	2.7~3.6	V
I2C Supply Voltage	I2CVDD	I2CVDD<IOVDD	1.65~3.6	V
MCLK Supply Voltage	MCLKVDD	MCLKVDD<IOVDD	1.65~3.6	V
GPIO Supply Voltage	GPIOVDD	GPIOVDD<IOVDD	1.65~3.6	V
Operating Temperature	Top	—	-20~+75	°C

Electrical Characteristics

DC Characteristics

(DVDD=DACVDD=ADCVDD=PLLVDD=2.25~2.50V, HPVDD=AVDD=IOVDD=2.7~3.6V,
I2CVDD=MCLKVDD=GPIOVDD=1.65~3.6V, Ta=-20~+75°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Related Pin
"H" Input Voltage 1	VIH1	GND=0V	I2CVDD×0.8 GPIOVDD×0.8 MCLKVDD×0.8	—	I2CVDD GPIOVDD MCLKVDD	V	*1
"L" Input Voltage1	VIL1	GND=0V	0	—	I2CVDD×0.2 GPIOVDD×0.2 MCLKVDD×0.2	V	
"H" Input Voltage2	VIH2	GND=0V	IOVDD×0.8	—	3.6	V	*2
"L" Input Voltage2	VIL2	GND=0V	0	—	IOVDD×0.2	V	
Clock input	Vckin	CKLRFOFF=1 Coupling Capacitor	0.4	—	—	Vpp	*3
"H" Output Voltage 1	VOH1	IOH=-1mA	I2CVDD×0.8 GPIOVDD×0.8 MCLKVDD×0.8	—	—	V	*4
"L" Output Voltage 1	VOL1	IOL=1mA	—	—	I2CVDD×0.2 GPIOVDD×0.2 MCLKVDD×0.2	V	
"L" Output Voltage 2	VOL2	IOL=20mA	—	—	IOVDD×0.25	V	*5
"H" Input leakage current	IIH	VI=VDD	—	—	10	μA	*6
"L" Input leakage current	IIL	VI=GND	-10	—	—	μA	
Operating Current 1	IDDO1	*7	—	8.5	13	mA	
Operating Current 2	IDDO2	*8	—	6.5	10	mA	
Operating Current 3	IDDO3	*9	—	1	2	mA	
Standby Current 1	IDDS1	-20~40°C	—	0.1	—	μA	
Standby Current 2	IDDS2	-20~50°C	—	0.5	15	μA	
Standby Current 3	IDDS3	-20~75°C	—	2	50	μA	

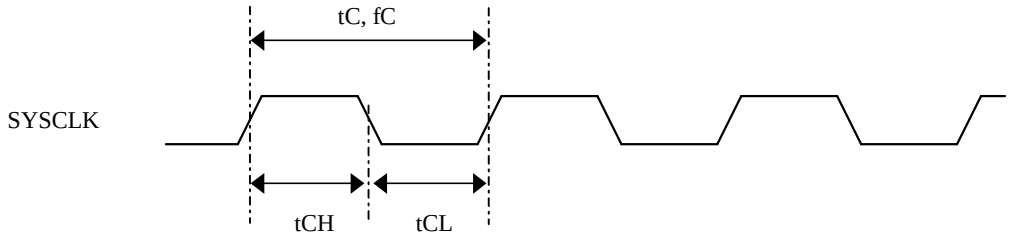
*1 Apply to input or input/output pin except I2C_SCL pin, I2C_SDA pin. Apply to SYSCLK pin (RFOFF="0").
*2 Apply to I2C_SCL pin, I2C_SDA pin.
*3 Apply to SYSCLK pin (RFOFF="1").
*4 Apply to output or input/output pin except I2C_SCL pin, I2C_SDA pin.
*5 Apply to I2C_SCL pin, I2C_SDA pin.
*6 Apply to all input or input/output pin.
*7 Apply to DVDD, DACVDD, ADCVDD, PLLVDD.
*8 Apply to HPVDD, AVDD, IOVDD.
*9 Apply to I2CVDD, MCLKVDD, GPIOVDD.

AC Characteristics

Clock

(DVDD=DACVDD=ADCVDD=PLLVDD=2.25~2.50V, HPVDD=AVDD=IOVDD=2.7~3.6V, I2CVDD=MCLKVDD=GPIOVDD=1.65~3.6V, Ta=-20~+75°C)

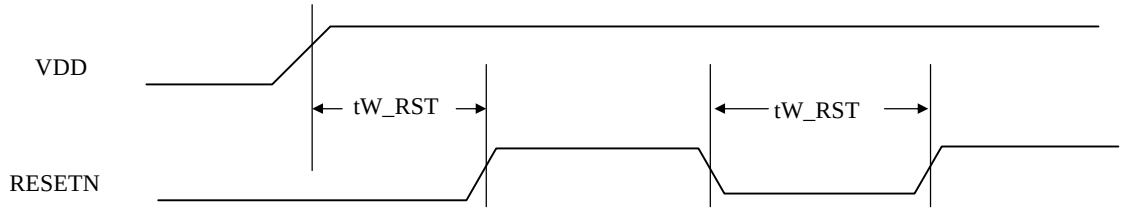
Parameter	Symbol	Min	Max.	Unit
SYSCLK Frequency	fC	8	20	MHz
SYSCLK Period	tC	1/fC	1/fC	ns
SYSCLK H Length	tCH	20	–	ns
SYSCLK L Length	tCL	20	–	ns



Reset

(DVDD=DACVDD=ADCVDD=PLLVDD=2.25~2.50V, HPVDD=AVDD=IOVDD=2.7~3.6V, I2CVDD=MCLKVDD=GPIOVDD=1.65~3.6V, Ta=-20~+75°C)

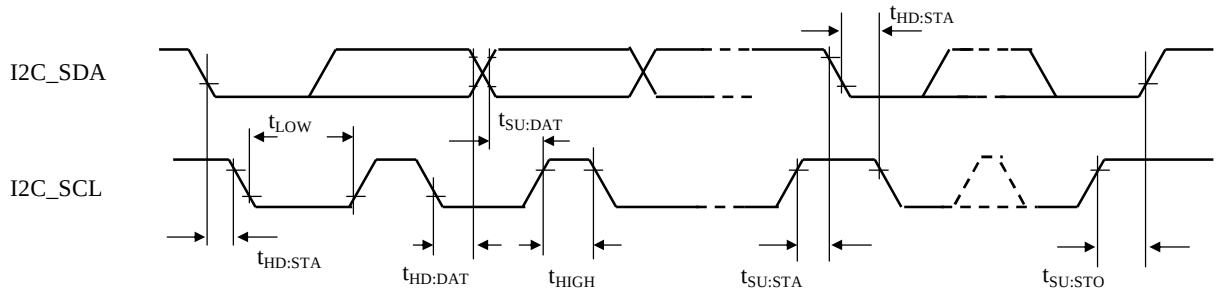
Parameter	Symbol	Min	Max.	Unit
RESETN Pulse Width	tW_RST	5	—	µs



I2C Interface

(DVDD=DACVDD=ADCVDD=PLLVDD=2.25~2.50V, HPVDD=AVDD=IOVDD=2.7~3.6V, I2CVDD=MCLKVDD=GPIOVDD=1.65~3.6V, Ta=-20~+75°C)

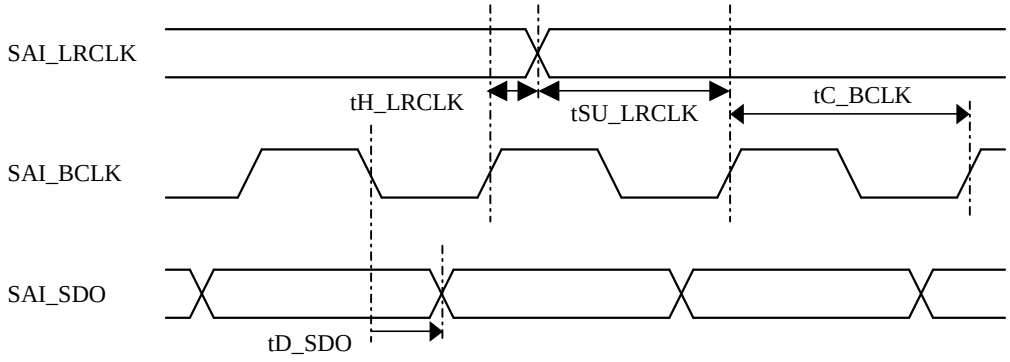
Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max.	Min	Max.	
I2C_SCL Frequency	f_{SCL}	—	100	—	400	kHz
I2C_SCL "L" Length	f_{LOW}	4.7	—	1.3	—	µs
I2C_SCL "H" Length	f_{HIGH}	4.0	—	0.6	—	µs
Hold time under Repeat [Start] Condition	$t_{HD:STA}$	4.0	—	0.6	—	µs
Setup Time under Repeat[Start] Condition	$t_{SU:STA}$	4.0	—	0.6	—	µs
Data Hold Time	$t_{HD:DAT}$	0	—	0	—	µs
Data Setup Time	$t_{SU:DAT}$	250	—	100	—	ns
Setup Time under [Stop] Condition	$t_{SU:STO}$	4.0	—	0.6	—	µs



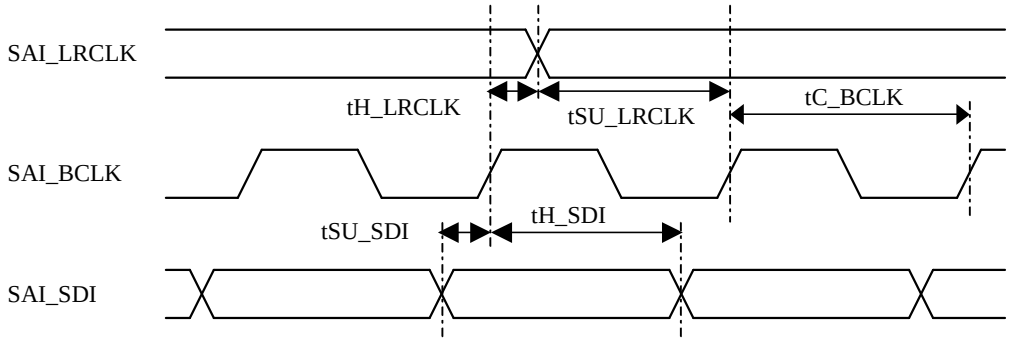
SAI (Slave)

(DVDD=DACVDD=ADCVDD=PLLVDD=2.25~2.50V, HPVDD=AVDD=IOVDD=2.7~3.6V, I2CVDD=MCLKVDD=GPIOVDD=1.65~3.6V, Ta=-20~+75°C)

Parameter	Symbol	Min	Max.	Unit
BCLK Period	tC_BCLK	—	128fs	Hz
LRCLK Hold Time	tH_LRCLK	20	—	ns
LRCLK Setup Time	tSU_LRCLK	20	—	ns
BCLK to DOut Delay Time	tD_SDO	—	70	ns
SDI Setup Time	tSU_SDI	20	—	ns
SDI Hold Time	tH_SDI	20	—	ns



SAI Transmit

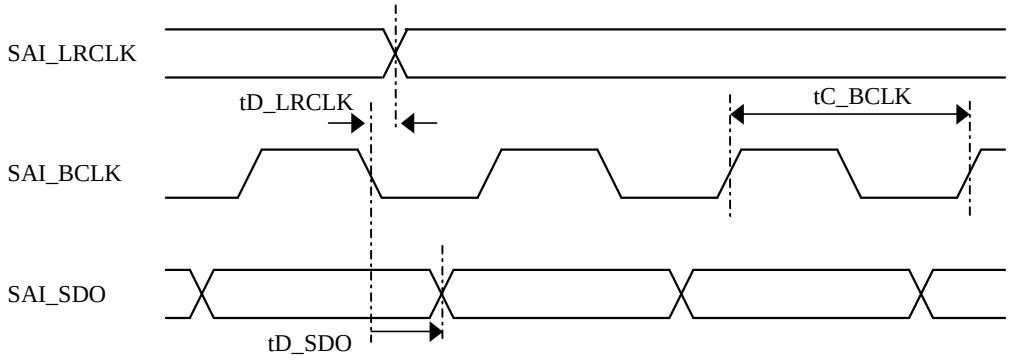


SAI Receive

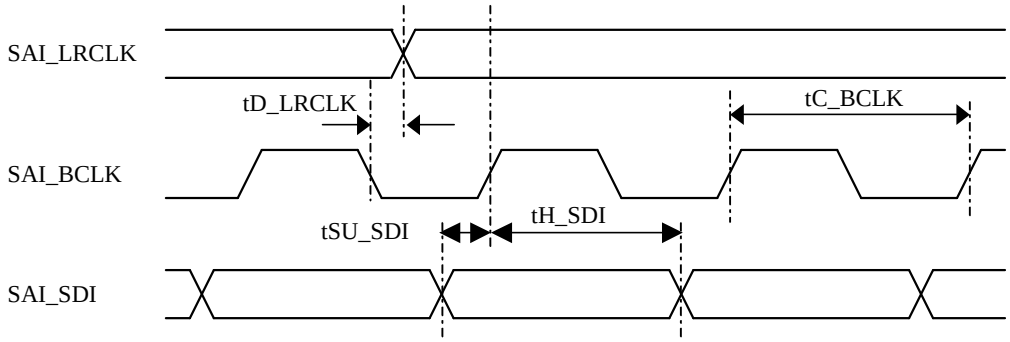
SAI (Master)

(DVDD=DACVDD=ADCVDD=PLLVDD=2.25~2.50V, HPVDD=AVDD=IOVDD=2.7~3.6V, I2CVDD=MCLKVDD=GPIOVDD=1.65~3.6V, Ta=-20~+75°C)

Parameter	Symbol	Min	Max.	Unit
BCLK Period	tC_BCLK	—	64fs	Hz
LRCLK Delay Time	tD_LRCLK	—	20	ns
BCLK to DOut Delay Time	tD_SDO	—	20	ns
SDI Setup Time	tSU_SDI	50	—	ns
SDI Hold Time	tH_SDI	0	—	ns



SAI Transmit

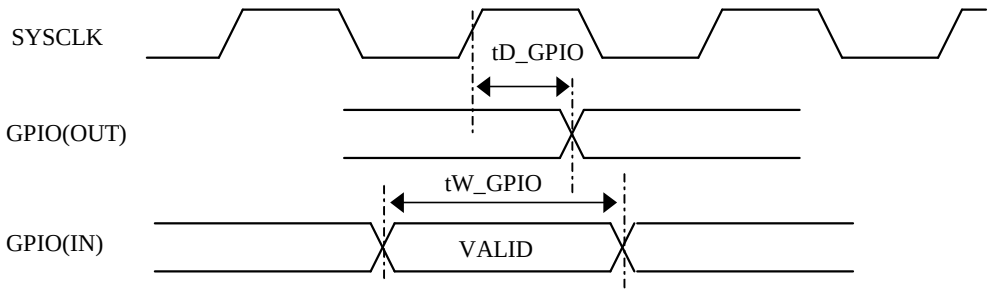


SAI Receive

GPIO

(DVDD=DACVDD=ADCVDD=PLLVDD=2.25~2.50V, HPVDD=AVDD=IOVDD=2.7~3.6V, I2CVDD=MCLKVDD=GPIOVDD=1.65~3.6V, Ta=-20~+75°C)

Parameter	Symbol	Min	Max.	Unit
GPIO Output Delay	tC_BCLK	—	64fs	Hz
GPIO Input Pulse Width	tD_LRCLK	—	20	ns

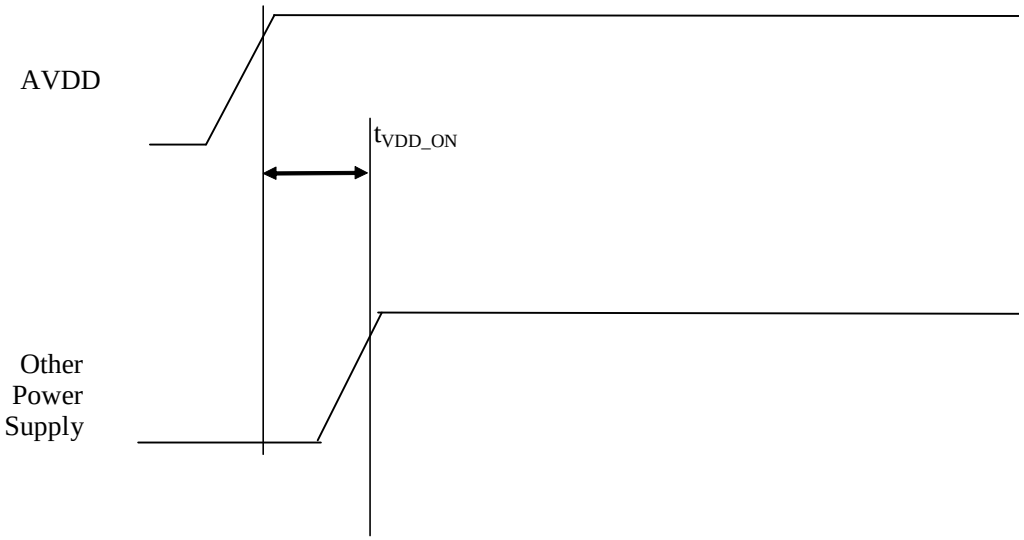


Power Supply Sequence

Please power on the LSI in the following sequence.

AVDD → Other Power SupplyPlease power on delay time less than 50ms from the AVDD turning on.

Parameter	Symbol	Min	Typ	Max	Unit
Power On Delay Time	t_{VDD_ON}	0	—	50	ms



Do not care power off the LSI.

Analog Characteristics

600Ω Line amplifier

AVDD=3V, ADCVDD=2.5V, Ta=25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Load Impedance	Rload		600	—	—	Ω
Playable Maximum Frequency	Fmax	Rload=600Ω	20	—	—	kHz

7kΩ Line amplifier

AVDD=3V, ADCVDD=2.5V, Ta=25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Load Impedance	Rload		7	—	—	kΩ
Playable Maximum Frequency	Fmax	Rload=7kΩ	20	—	—	kHz

Receiver amplifier

HPVDD=3V, ADCVDD=2.5V, Ta=25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Load Impedance	Rload		32	—	—	Ω
Playable Maximum Frequency	Fmax	Rload=32Ω, -3dB	20	—	—	kHz

Headphone amplifier

HPVDD=3V, ADCVDD=2.5V, Ta=25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Load Impedance	Rload		32	—	—	Ω
Playable Maximum Frequency	Fmax	Rload=32Ω, -3dB	20	—	—	kHz

ADC

AVDD=3V, ADCVDD=2.5V, Ta=25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resolution	ADb		—	16	—	bit
S/(N+D)	ADsnd1	1kHz, 0dB FS	—	82	—	dB

DAC

AVDD=3V, DACVDD=2.5V, Ta=25°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resolution	DAb		—	16	—	bit
S/(N+D)	DAsnd1	1kHz, 0dB FS	—	84	—	dB

Revision History

Date	Page	Notes	Revision
05/12/09	All	Release first version	1.0.0

NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.
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