ML2601 DATASHEET

Version 2.00.00
Revised on 27-Dec-05

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Contents

General Description

The ML2601 is a high quality 3D surround enhancement LSI for audio applications, based on SRS Labs WOW XT™ technology. The LSI supports two modes, SRS3D Headphone and SRS3D Extreme, with emphasis on low power through a complete hardwired solution. The ML2601 also incorporates an 8Ω stereo speaker amplifier. Typical applications are mobile phones and portable audio players.

Features

1) 3D surround powered by SRS Lab
   - SRS3D headphone: high quality 3D surround for headphone
   - SRS3D (Extreme mode): high quality 3D surround for speakers in mobile phone

2) 8Ω stereo speaker amplifiers
   - BTL 650mW drive

3) CPU I/F
   I2C slave mode
   - 7bit addressing, address 1bit is changeable by pin
   - Support Standard / Fast mode

4) Serial Audio Interface (SAI)
   - Sampling frequency 16k ,22.05k, 24k, 32k, 44.1k, 48k Hz
   - Channel data length: 16bit
   - Support only slave mode
   - LRCLK positive/negative selectable
   - Support MSB first 1bit delay mode and Left Justified mode
   - Serial Clock: 32clock-128clock

5) PCM Interface
   - Support 4slot (input 2slot, output 2slot)

6) Clock
   - 13MHz and 26MHz

7) Package
   Package size: 3.19mm×2.56mm
   0.5mm pitch 30pin W-CSP

Block Diagram

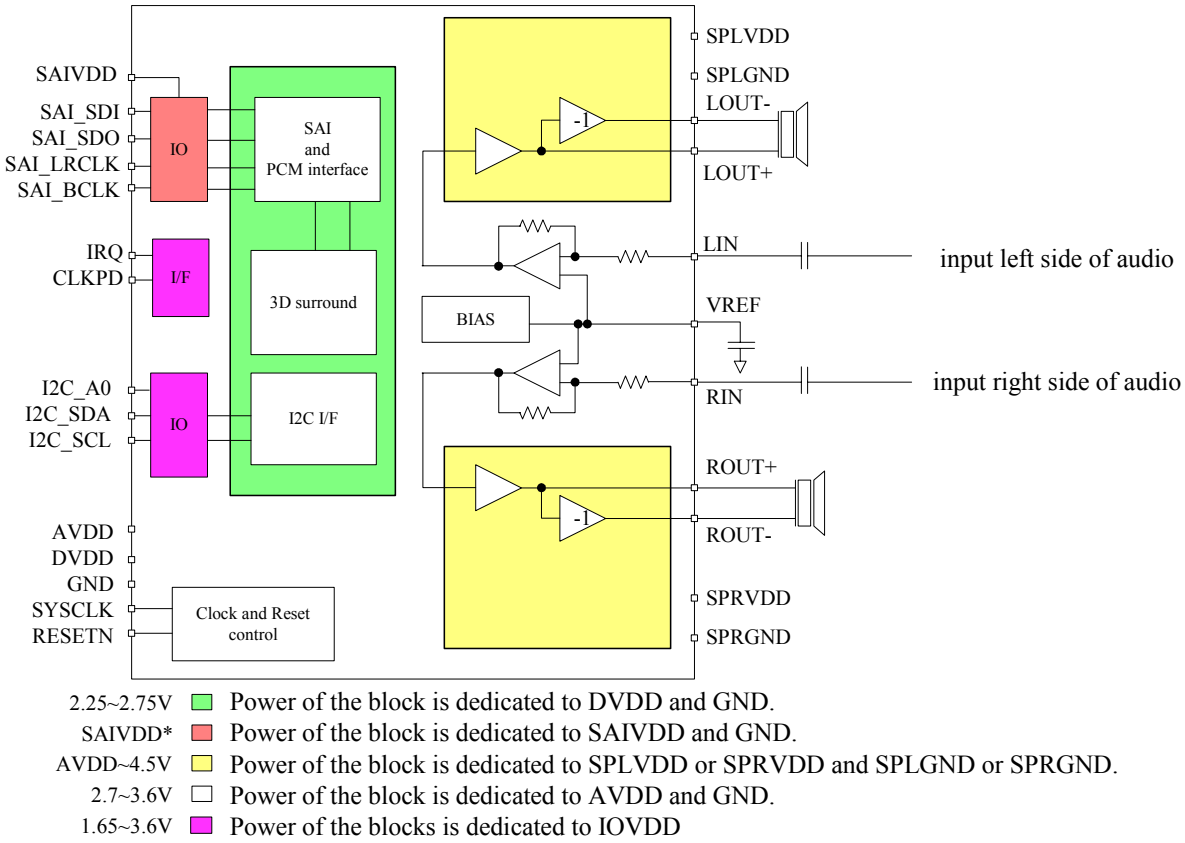


Fig.1 Block Diagram

SAI : Serial Audio Interface
I2C : CPU Interface
IO : Input and Output buffer
BIAS : Reference voltage for analog block

*: 1.65-3.6V: in SAI mode
1.71-1.89V, 2.65-2.85V: in PCM mode

Application Example

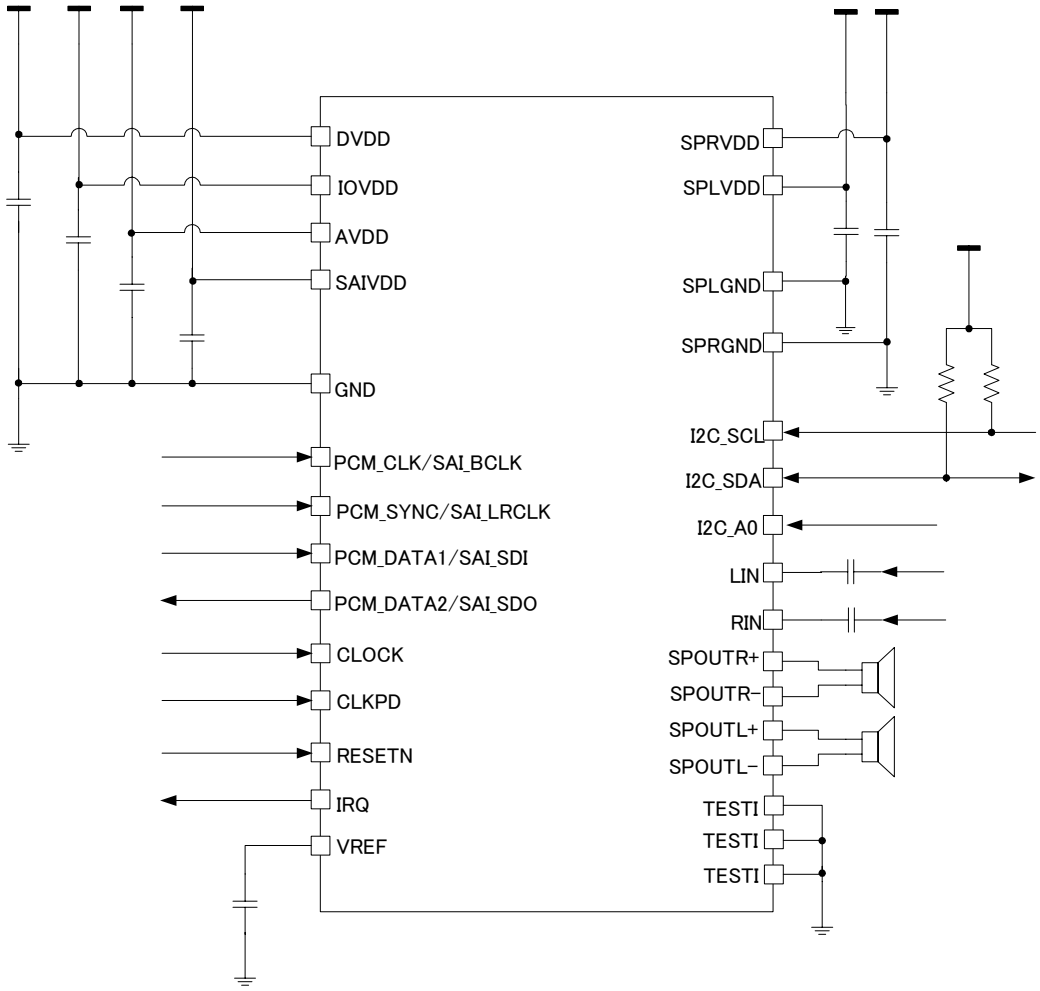


Fig.2 Application example

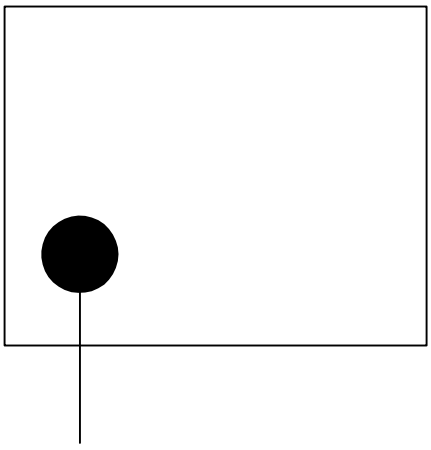
Pin Layout

Bottom View

	F	E	D	C	B	A
5	DVDD	I2C_A0	I2C_SCL	RESETN	GND	SAI_SDO
4	AVDD	CLOCK	I2C_SDA	IOVDD	SAI_BCLK	SAIVDD
3	LIN	CLKPD	IRQ	TESTI	SAI_LRCLK	RIN
2	SPLVDD	TESTI	VREF	TESTI	SAI_SDI	SPRVDD
1	SPLGND	SPOUTL+	SPOUTL-	SPOUTR-	SPOUTR+	SPRGND

Fig.3 Pin Layout

Top View



Pin A1

Pin Description

	Name	IO	Power	Description
A1	SPRGND	P		GND
A2	SPRVDD	P		Power for SP Amp Rch
A3	RIN	I		Audio input Rch
A4	SAIVDD			Power for PCM Interface
A5	SAI_SDO (PCM_DATA2)	IO	SAIVDD	Serial data output (PCMDat-B for PCM in PCM mode)
B1	SPOUTR+	O	SPRVDD	R-ch BTL Speaker Amp output.
B2	SAI_SDI (PCM_DATA1)	IO	SAIVDD	Serial data input (PCMDat-A for PCM in PCM mode)
B3	SAI_LRCLK (PCM_SYNC)	I I	SAIVDD	LR clock input (FrameSYNC for PCM in PCM mode)
B4	SAI_BCLK (PCM_CLK)	I I	SAIVDD	Clock input (PCM CLOCK for PCM in PCM mode)
B5	GND	P	-	GND (for AVDD, SAIVDD, DVDD,IOVDD)
C1	SPOUTR-	O	SPRVDD	R-ch BTL Speaker Amp output.
C2	TESTI	IO		For test(Please connect to GND level)
C3	TESTI	IO		For test(Please connect to GND level)
C4	IOVDD	P		Power Supply for IO pin; (I2C, IRQ, CLKPD, RESETN)
C5	RESETN	I	IOVDD	LSI reset input
D1	SPOUTL-	O	SPRVDD	L-ch BTL Speaker Amp output.
D2	VREF	O	AVDD	Reference voltage output for VBG. Need to connect 1uF capacitor to GND.
D3	IRQ	O	IOVDD	Interrupt output Outputs “H” level, When occurred interrupt. When set ISS bit of the INTERRUPT ENABLE register to “0”, the polarity of the interrupt is inverted.
D4	I2C_SDA	IO	IOVDD	I2C bus data input/output
D5	I2C_SCL	IO	IOVDD	I2C bus clock input
E1	SPOUTL+	O	SPLVDD	L-ch BTL Speaker Amp output.
E2	TESTI	IO	-	For test(Please connect to GND level)
E3	CLKPD	I	IOVDD	Clock buffer disable control
E4	CLOCK	I	AVDD	System clock
E5	I2C_A0	I	IOVDD	Set I2C slave address
F1	SPLGND	P		GND
F2	SPLVDD	P		Power for SP AMP Lch
F3	LIN	I	AVDD	Audio input Lch
F4	AVDD	P		Analog Power
F5	DVDD	P		Core digital Power

Absolute Maximum Ratings

	Symbol	Condition	Rating	Unit
Core Supply Voltage	DVDD	—	-0.3～3.6	V
PCM I/F Supply Voltage	SAIVDD	—	-0.3～4.5	V
IO Supply Voltage	IOVDD	—	-0.3～4.5	V
SPAMP（Lch） Supply Voltage	SPLVDD	—	-0.3～5.5 *5	V
SPAMP（Rch） Supply Voltage	SPRVDD	—	-0.3～5.5 *5	V
Analog Supply Voltage	AVDD	—	-0.3～4.5	V
Input Voltage	Vin	*1	-0.3～AVDD+0.3	V
		*2	-0.3～IOVDD+0.3	V
		*3	-0.3～SAIVDD+0.3	V
Output Current	Io	*4	-8 ～ +8	mA
Storage Temperature	Tstg	—	-55～+125	℃
Power Dissipation	Pd	—	Refer to section of “Power Derating Curves”	W

*1 SYSCLK,LIN,RIN
*2 I2C_SCL, I2C_SDA,I2C_A0,RESETN,CLKPD,IRQ.
*3 SAI_BCLK, SAI_LRCLK, SAI_SDI, SAI_SDO.
*4 Applies to all output and in/output pins except for SPOUTL+/- and SPOUTR+/-.
（I2C_SCL, I2C_SDA, I2C_A0, IRQ, SAI_BCLK, SAI_LRCLK, SAI_SDI, SAI_SDO）
*5 Lch and Rch supply voltage must be the same level
Note）Do not short the output pin to another output pin, power supply or GND.
（Output pin includes an I/O pin which is in output mode）

Recommended Operating Condition

Parameter	Symbol	Condition	Rating	Unit
Core Supply Voltage	DVDD	DVDD＜=AVDD GND=SPLGND=SPRGND=0	2.25～2.75	V
PCM I/F Supply Voltage	SAIVDD	GND=SPLGND=SPRGND=0 PCM mode	1.71～1.89 2.65～2.85	V
		GND=SPLGND=SPRGND=0 I2S mode	1.65～3.6	V
IO Supply Voltage	IOVDD	GND=SPLGND=SPRGND=0	1.65～3.6	V
SPAMP（Lch） Supply Voltage*	SPLVDD	SPLVDD=SPRVDD, GND=SPLGND=SPRGND=0	AVDD～4.5	V
SPAMP（Rch） Supply Voltage*	SPRVDD	SPLVDD=SPRVDD, GND=SPLGND=SPRGND=0	AVDD～4.5	V
Analog Supply Voltage	AVDD	GND=SPLGND=SPRGND=0	2.7～3.6	V
Operating Temperature	Ta	—	-20～+85 （Tjmax=125）	℃

* Lch and Rch supply voltage must be the same level.

Electrical Characteristics

DC Characteristics

Ta=-20～85℃
(DVDD=2.25 to 2.75, SAIVDD=1.65 to 3.6, IOVDD=1.65 to 3.6, AVDD=2.7 to 3.6, SPLVDD=SPRVDD=AVDD to 4.5)

Parameter	Symbol	Condition	Min.	Typ. *	Max.	Unit	Related Pin
“H” Input Voltage 1	VIH1	GND=0V	IOVDD×0.8	—	IOVDD	V	*1
“L” Input Voltage 1	VIL1	GND=0V	0	—	IOVDD×0.2	V	*2
“H” Input Voltage 2	VIH2	GND=0V	AVDD×0.8	—	AVDD	V	*4
“L” Input Voltage 2	VIL2	GND=0V	0	—	AVDD×0.2	V	
“H” Input Voltage 4	VIH4	GND=0V	IOVDD×0.8	—	3.6	V	*6
“L” Input Voltage 4	VIL4	GND=0V	0	—	IOVDD×0.2	V	
“H” Input Voltage 5	VIH5	SAIVDD=1.71～1.89V GND=0V	SAIVDD×0.72	—	SAIVDD	V	*7
“L” Input Voltage 5	VIL5	SAIVDD=1.71～1.89V GND=0V	—	—	SAIVDD×0.25	V	
“H” Input Voltage 3	VIH3	GND=0V	SAIVDD×0.8	—	SAIVDD	V	*8
“L” Input Voltage 3	VIL3	GND=0V	0	—	SAIVDD×0.2	V	
Schmitt trigger hysteresis 1	Vh1	GND=0V	IOVDD×0.1	—	—	V	*2
Clock input	Vckin		0.4	—	—	Vpp	*3
“H” Output Voltage 1	VOH1	IOH=-1mA	IOVDD×0.8	—	—	V	*5
“L” Output Voltage 1	VOL1	IOL=1mA	—	—	IOVDD×0.2	V	
“L” Output Voltage 2	VOL2	IOL=20mA	—	—	IOVDD×0.25	V	*6
“L” Output Voltage 3	VOL3	IOL=4mA	0		SAIVDD x 0.22	V	*7
“H” Output Voltage 3	VOH3	IOH=-4mA	SAIVDD x 0.8		SAIVDD	V	*7
“L” Output Voltage 4	VOL4	IOL = 100uA	0		0.20	V	*7
“H” Output Voltage 4	VOH4	IOH = -100uA	SAIVDD – 0.2		SAIVDD	V	*7
Output leakage current	IOZ	Vi<VIL5 Vo = Hi Z	-1		1	uA	*7
“H” Input leakage current	IIH1	VI=VDD	—	—	10	uA	
“L” Input leakage current	IIL1	VI=GND	-10	—	—	uA	
Operating Current	IDDO	*9	—	15	40	mA	
Standby Current	IDDS	Ta<=+40℃ Ta<=+85℃	— —	1 —	10 100	uA uA	

*1 CLKPD, I2C_A0
*2 RESETN
*3 SYSCLK(CLKRFOFF=”0”)
*4 SYSCLK(CLKRFOFF=”1”)
*5 IRQ
*6 I2C_SCL, I2C_SDA
*7 PCM mode : PCM_CLK, PCM_SYNC, PCM_DATA1, PCM_DATA2
*8 SAI mode : SAI_BCLK, SAI_LRCLK, SAI_SDI, SAI_SDO
*9 No load at Speaker output
* The “Typ.” values are reference value, It is not be guaranteed.

AC Characteristics

Clock

Ta=-20 to 85℃
(DVDD=2.25 to 2.75, SAIVDD=1.65 to 3.6, IOVDD=1.65 to 3.6, AVDD=2.7 to 3.6, SPLVDD=SPRVDD=AVDD to 4.5)

Parameter	Symbol	Min	Typ.	Max.	Unit
CLOCK Frequency	fC	12.35	13	13.65	MHz
		24.7	26	27.3	MHz
CLOCK Period	tC	1/fC		1/fC	ns
CLOCK H Length	tCH	0.4 X tC		—	ns
CLOCK L Length	tCL	0.4 X tC		—	ns

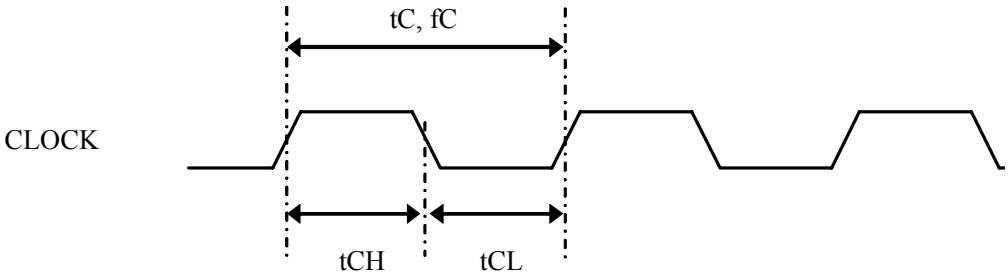
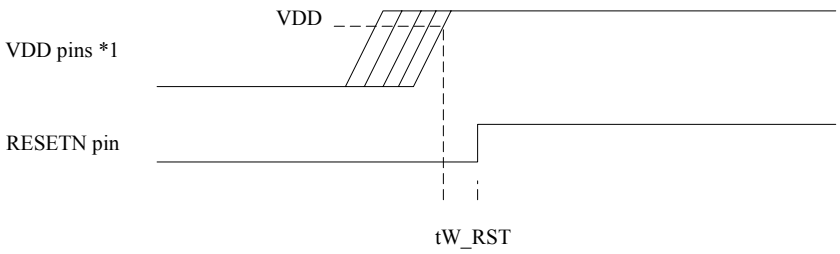


Fig.4 Clock timing

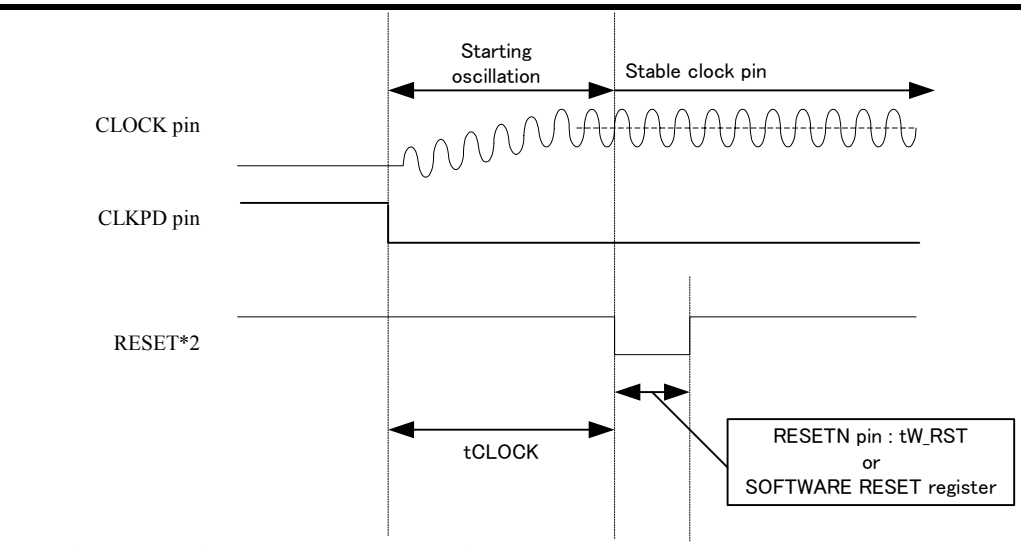
Reset

Ta=-20 to 85℃
(DVDD=2.25 to 2.75, SAIVDD=1.65 to 3.6, IOVDD=1.65 to 3.6, AVDD=2.7 to 3.6, SPLVDD=SPRVDD=AVDD to 4.5)

Parameter	Symbol	Min	Max.	Unit	Note
RESET Pulse Width	tW_RST	5	—	us	
Stabilizing Clock time	tCLOCK	0	500	ms	Depend on external coupling C value
CLOCK Periods	tC	—	80.97	ns	



VDD pins *1: Please reset LSI, after power supply all VDD pins



RESET*2: RESETN pin or SOFTWARE RESET register

Fig.5 Reset timing

I2C Interface

Ta=-20 to 85℃
(DVDD=2.25 to 2.75, SAIVDD=1.65 to 3.6, IOVDD=1.65 to 3.6, AVDD=2.7 to 3.6, SPLVDD=SPRVDD=AVDD to 4.5)

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max.	Min	Max.	
I2C_SCL Frequency	f_{SCL}	–	100	–	400	KHz
I2C_SCL "L" Length	f_{LOW}	4.7	–	1.3	–	us
I2C_SCL "H" Length	f_{HIGH}	4.0	–	0.6	–	us
Hold time under Repeat [Start] Condition	$t_{HD:STA}$	4.0	–	0.6	–	us
Setup Time under Repeat[Start] Condition	$t_{SU:STA}$	4.7	–	0.6	–	us
Data Hold Time	$t_{HD:DAT}$	0	–	0	–	us
Data Setup Time	$t_{SU:DAT}$	250	–	100	–	ns

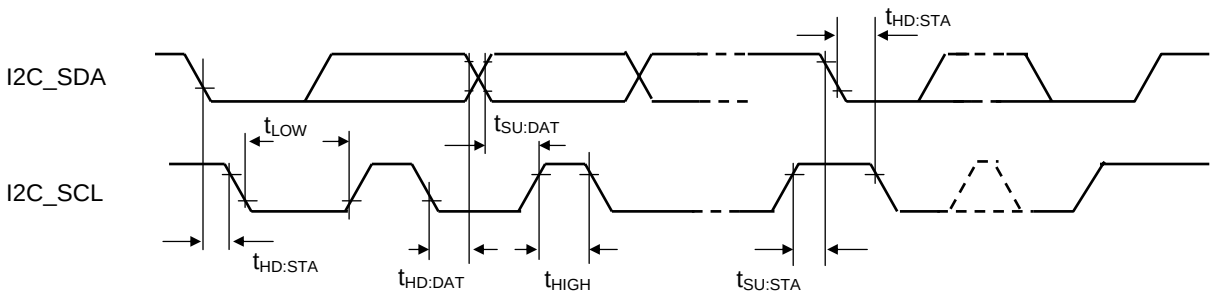
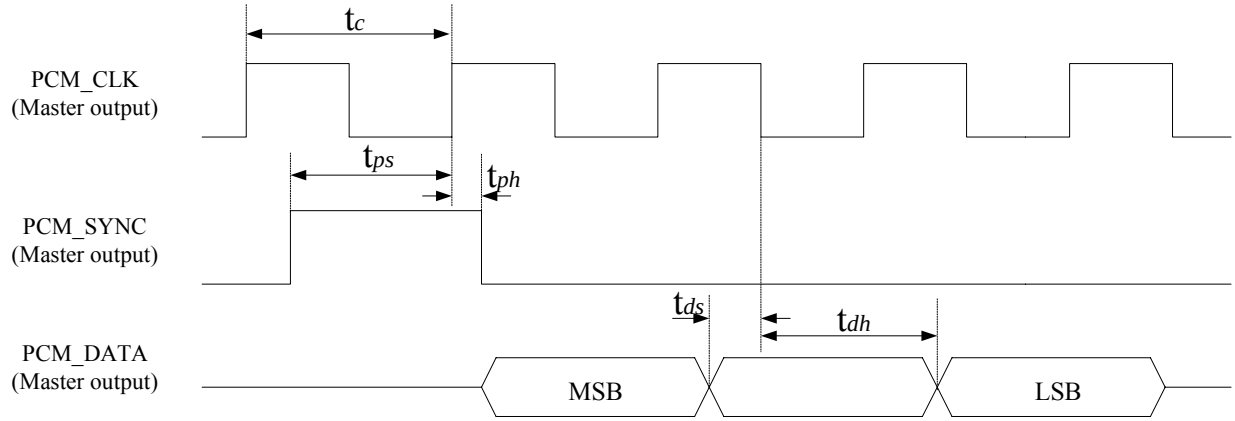


Fig.6 I2C Timing

PCM Interface

The timing characteristics are illustrated in the following diagram (fig.7). The fastest PCM clock is 6.1MHz with a 50% duty cycle.

Receive data



Transmit data

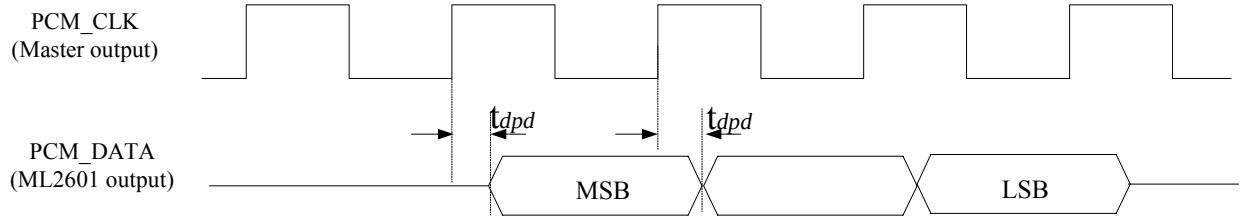


Fig.7 PCM timing

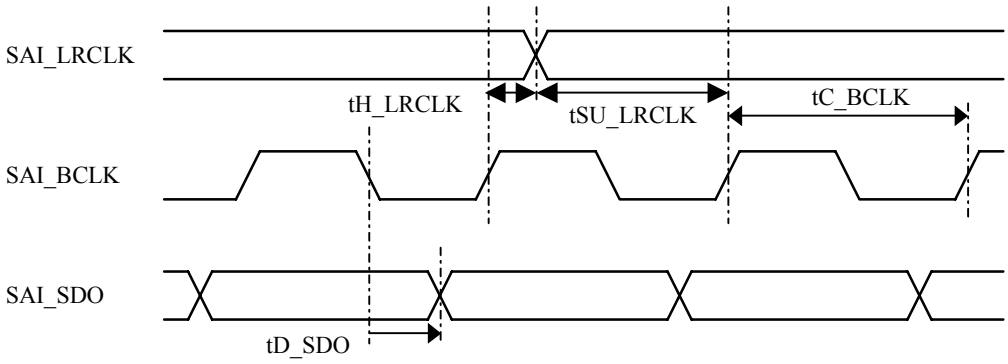
Ta=-20 to 85℃
(DVDD=2.25 to 2.75, SAIVDD=1.71 to 1.89, IOVDD=1.65 to 3.6,
AVDD=2.7 to 3.6, SPLVDD=SPRVDD=AVDD to 4.5)

Slave Parameters	Symbol	Min	Max	Unit
PCM_CLK period time (f_{max} of PCMCLK = 6.1 MHz)	t_c	163	---	ns
PCM_SYNC input setup time to falling edge of PCMCLK	t_{ps}	108.5	---	ns
PCM_SYNC input hold time to falling edge of PCMCLK	t_{ph}	38	---	
PCM_DATA output valid after rising edge of PCMCLK (Load condition:Cload=50pF)	t_{dpd}	0	35	ns
PCM_DATA input setup time to falling edge of PCMCLK	t_{ds}	65	---	ns
PCM_DATA input hold time to falling edge of PCMCLK	t_{dh}	81.5	---	ns

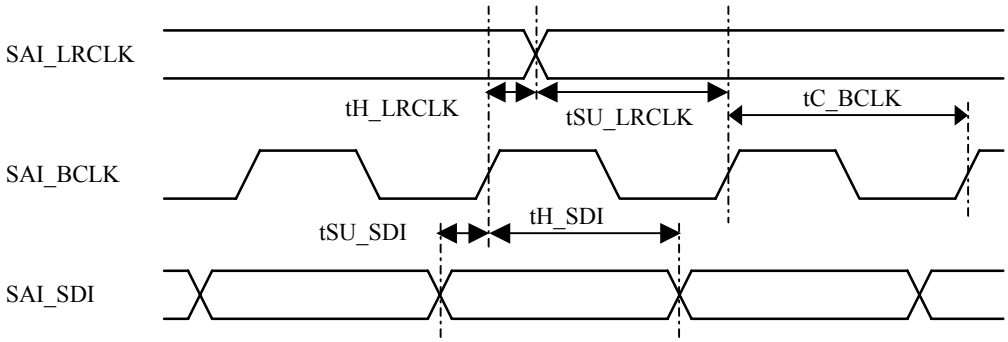
SAI

Ta=-20 to 85℃
(DVDD=2.25 to 2.75, SAIVDD=1.65 to 3.6, IOVDD=1.65 to 3.6, AVDD=2.7 to 3.6, SPLVDD=SPRVDD=AVDD to 4.5)

Parameter	Symbol	Min	Max.	Unit
BCLK period	tC_BCLK	–	128fs	Hz
LRCLK Hold	tH_LRCLK	20	–	ns
LRCLK Setup	tSU_LRCLK	20	–	ns
BCLK to DOut delay	tD_SDO	–	70	ns
SDI Setup	tSU_SDI	20	–	ns
SDI Hold	tH_SDI	20	–	ns



SAI Transmit



SAI Receive

Fig.8 SAI timing

Power Supply Sequence

Please Power on the LSI in the following sequence.
SPLVDD,SPRVDD → AVDD → IOVDD → SAIVDD → DVDD

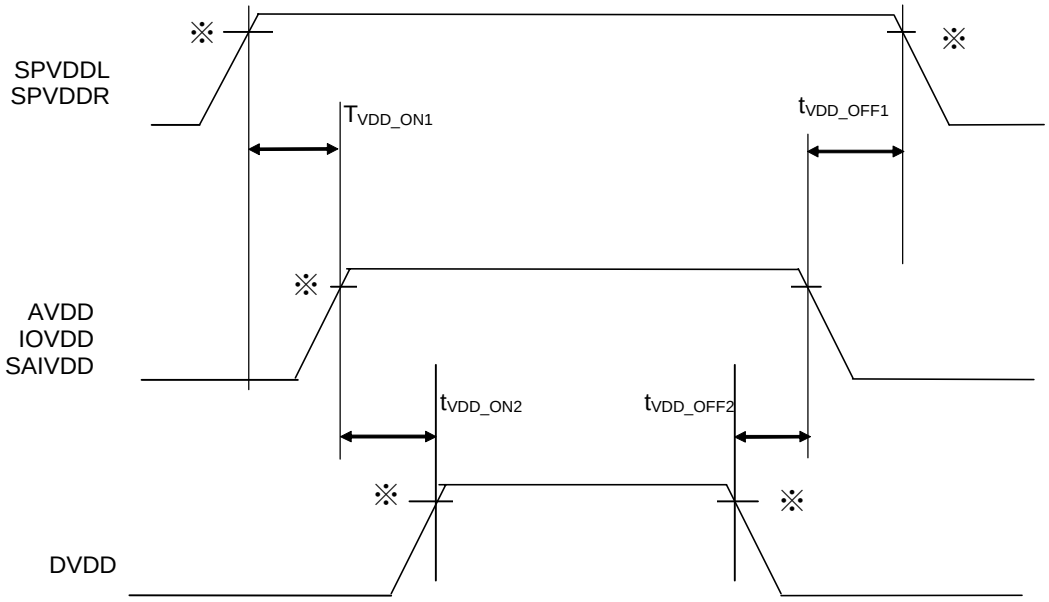
Please Power Off the LSI in the following sequence.
DVDD → SAIVDD→ IOVDD → AVDD→ SPLVDD,SPRVDD

ML2601 power supply (AVDD, IOVDD, SAIVDD and DVDD) is only allowed under the following two conditions:

1) All four power supplies are in the turned on state..
2) All four power supplies are in the turned off state.

Ta=-20 to 85℃
(DVDD=2.25 to 2.75, SAIVDD=1.65 to 3.6, IOVDD=1.65 to 3.6, AVDD=2.7 to 3.6, SPLVDD=SPRVDD=AVDD to 4.5)

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Power On delay time 1	t_{VDD_ON1}	—	0	—	—	ms	
Power On delay time 2	t_{VDD_ON2}		0	—	100	ms	
Power Off delay time 1	t_{VDD_OFF1}		0	—	—	ms	
Power Off delay time 2	t_{VDD_OFF2}		0	—	100	ms	



※ each supply voltage is the minimum value

Fig.9 Power supply sequence

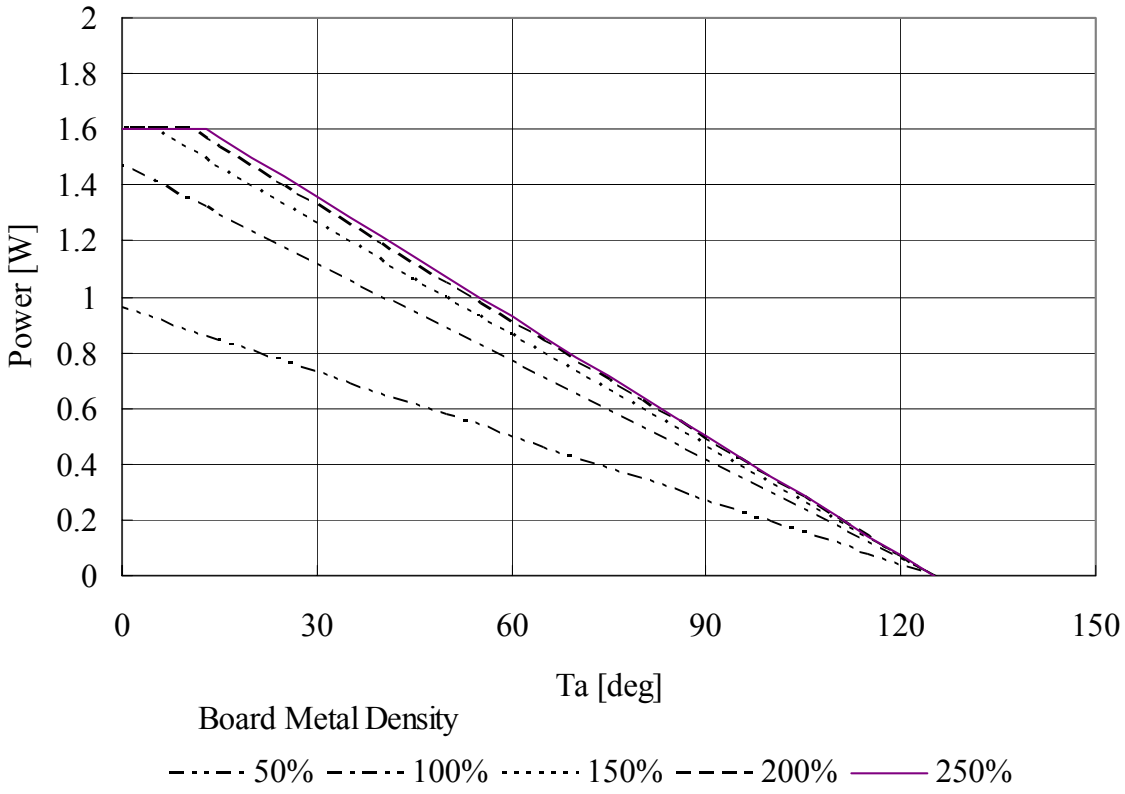
Analog Characteristics

Speaker amplifier characteristics

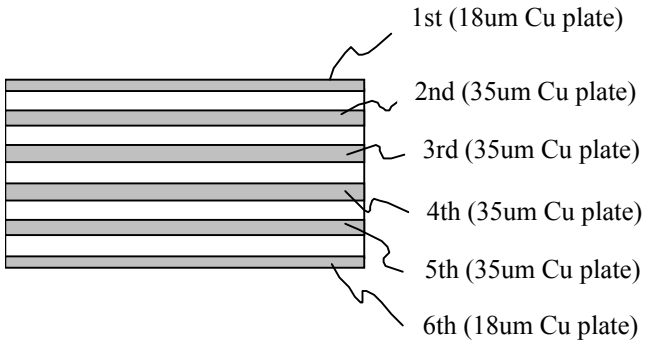
(Ta=25℃)
(DVDD=2.25 to 2.75, SAIVDD=1.65 to 3.6, IOVDD=1.65 to 3.6, AVDD=2.7 to 3.6, SPLVDD=SPRVDD=3.6)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Load Impedance	Rload	SPOUTR+,SPOUTR- SPOUTL+, SPOUTL-	8	—	—	Ω
Playable Maximum Frequency	Fmax	No load	20	—	—	kHz
Input Resistance	Rin	RIN, LIN	—	35	—	kΩ

Power Derating Curves



●Board Structure



Simulation Condition						
Board Metal Density	1st	2nd	3rd	4th	5th	6th
50%	50%	-	-	-	-	-
75%	75%	-	-	-	-	-
100%	50%	50%	-	-	-	-
150%	50%	100%	-	-	-	-
200%	50%	100%	50%	-	-	-
250%	50%	100%	100%	-	-	-

Functional Description

Clock

Following Figure shows the functional block diagram of the clock input.

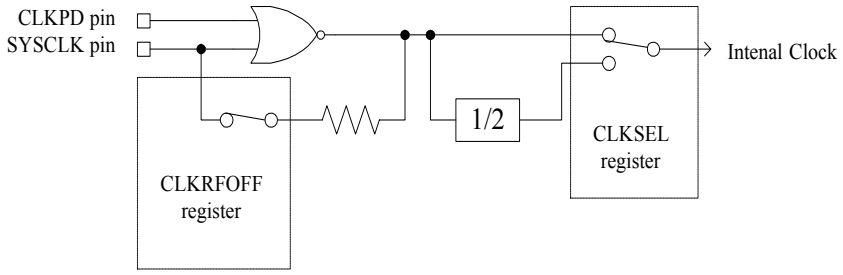


Fig.10 Clock Diagram

-Input clock frequency

The ML2601 supports two input clock frequencies: 13MHz and 26MHz.

Since the working frequency inside LSI is 13MHz, enabling of the clock divide circuit is dependant on the input clock frequency.

Setting the DIVSEL bit in the Clock Select Register will divide the input clock.

- Input clock amplitude

Input clock amplitude is permitted from 0.4Vpp to Full Swing. Conditions are as follows:

- If the High level and Low level of the clock amplitude is VIH and VIL there is no need to connect a coupling capacitor to the clock input pin.
- If the clock amplitude is below the specified range the ML2601 needs its clock input via a coupling capacitor.
- If the amplitude of the clock is small the RFOFF bit should be set to '0' in the Clock Feedback Resistor Control Register.

The table below shows the relationship between the coupling capacitor value and the stabilizing time of the on-board clock.

Coupling Capacitor	CLOCK stabilizing time tCLOCK (ms)	Register setting
no	0	CLKRFOFF="1"
100pF	0.5	CLKRFOFF="0"
1000pF	5	CLKRFOFF="0"
0.01uF	50	CLKRFOFF="0"
0.1uF	500	CLKRFOFF="0"

- Related register

Clock Select register

Clock Feedback Resistor Control register

Reset

Since an anti-noise filter is embedded within the LSI in order to avoid the wrong resetting, please input RESET signal with at least a 5 μ s pulse width.

Serial Audio Interface and PCM Interface

There are two types of Audio Interface inside the LSI. One is General 4 lines digital PCM data transferring interface SAI (Serial Audio Interface). The other is original PCM interface which is proprietary PCM interface. Both interfaces use the same sets of pins. In order to choose one of the two interfaces, please set the SAI bit in the SAI/PCM Interface Select Register

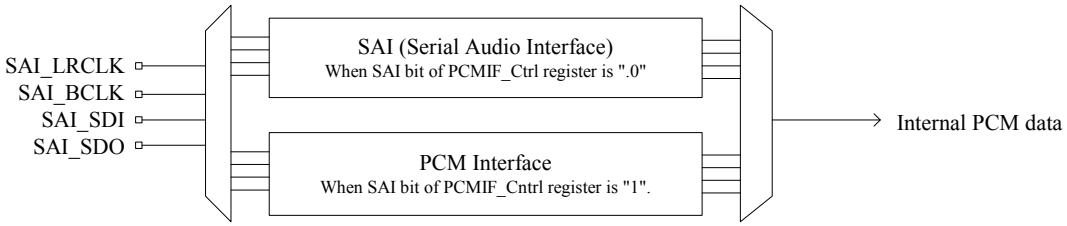
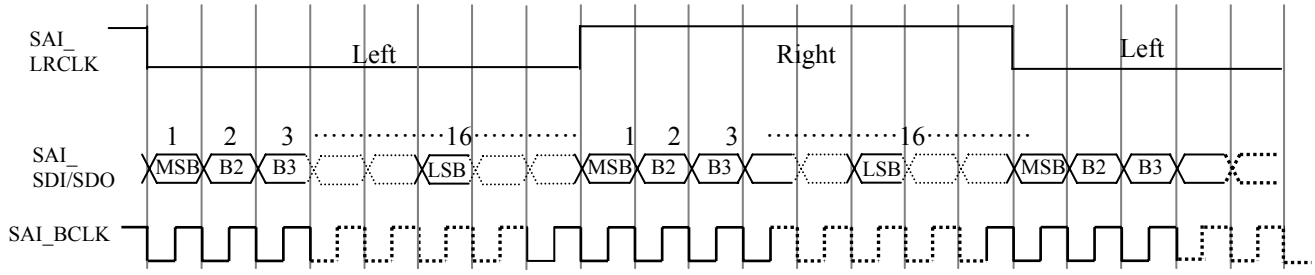


Fig.11 SAI I/F and PCM I/F

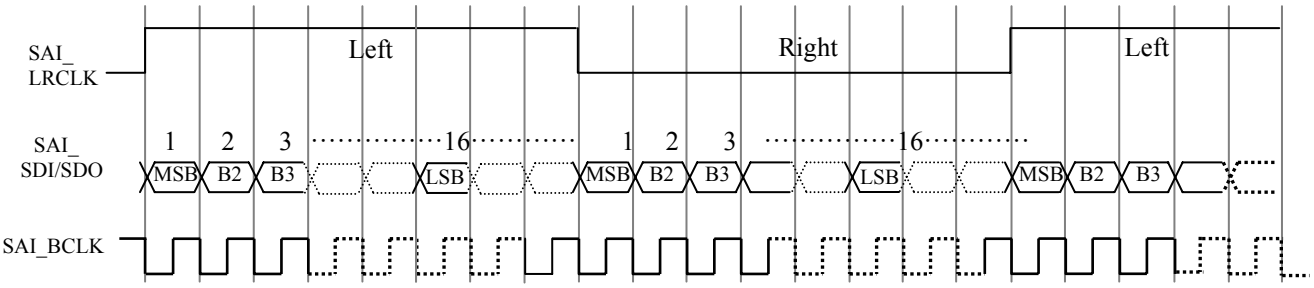
- Related register
  SAI Control Register

- SAI Interface
  The LSI supports four formats in SAI mode, in accordance with SAI control register settings.

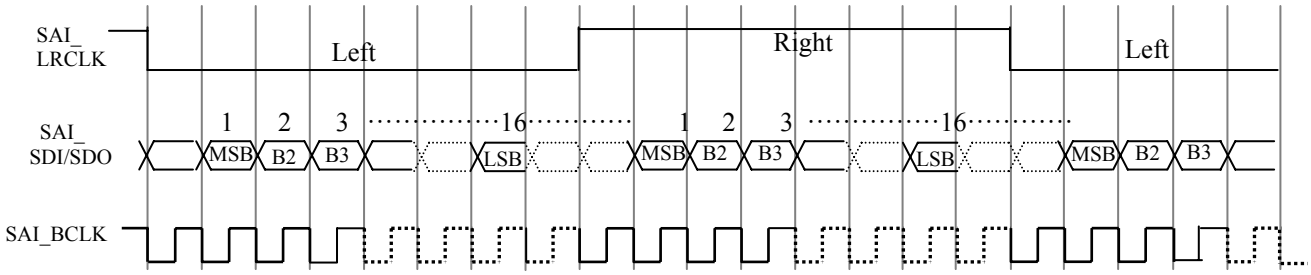
Left Justified Mode: DLYO bit and DLYI bit of SAICON0 register = “0”
WSL=”0”、 DLYO/1=”0”



WSL=”1”、 DLYO/1=”0”



Left Justified Mode: DLYO bit and DLYI bit of SAICON0 register = “0”
WSL=”0”、 DLYO/1=”1”



WSL=”1”、 DLYO/1=”1”

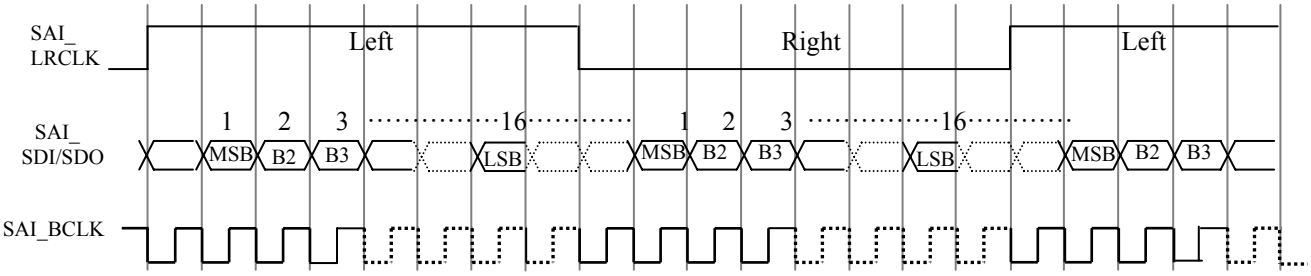


Fig.12 SAI timing Chart

- PCM Interface
  The LSI supports following timings in PCM interface mode.
  Direction of PCM_DATA0 pin and PCM_DATA1 and number of slots are programmable.

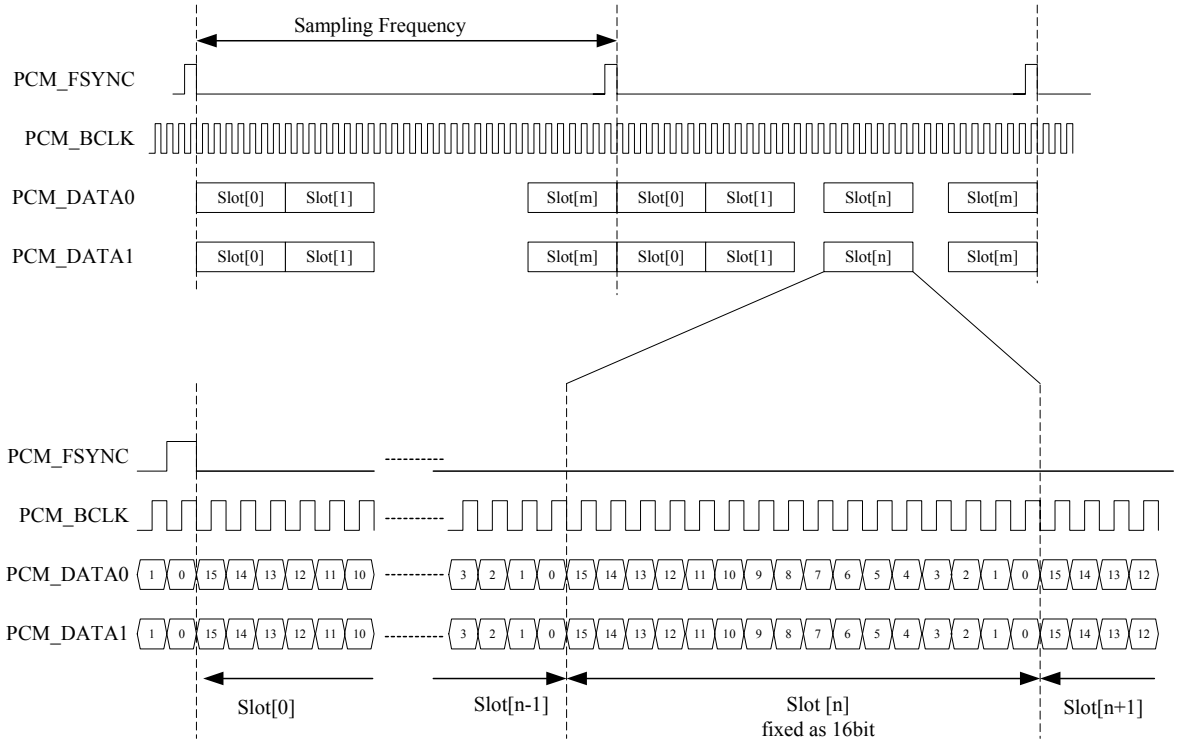


Fig13. PCM timing

I2C Interface

ML2601 has the serial interface, which complies with I2C bus standards. It operates as an I2C slave. The high 6 bits of the LSI address are fixed at “001100”. LSB is changed via I2C_A0 Pin.

- I2C format

Write

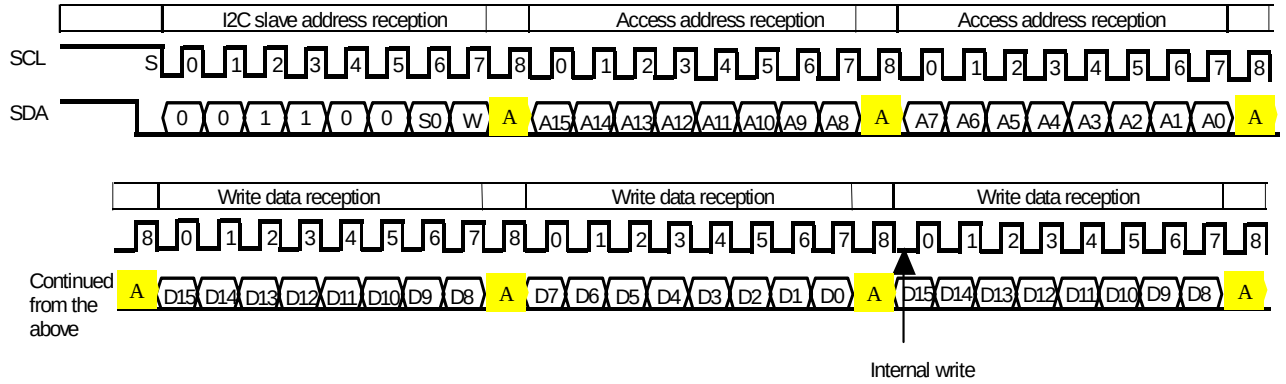


Fig.14 I2C Write Format

After the LSI writes data (Fig.14 Internal Write), if there is no Stop or Restart condition input when the SCL is “H”, it will be looked as writing continuously and the next received 16 bits of data will be written. The on-board address counter will then increment by 0x02h.

Read

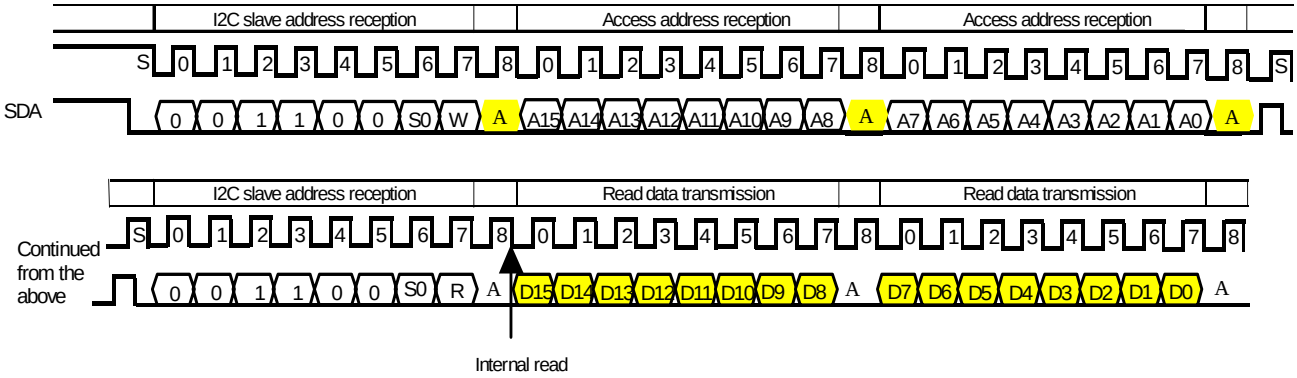


Fig.15 I2C Read Format

If the Master response to the 16 bit data transferred from ML2601 is ACK, it will be considered as reading continuously. The address counter within the ML2601 will be incremented by 0x02h. The data from the address will be read and the LSI will prepare for the next 16 bits of data to be transferred.

Note: The yellow part in the picture above shows the I2C Bus driven by ML2601.

3D surround

The ML2601 provides high quality 3Dsurround sound enhancement powered by SRS Labs. The LSI incorporates two technologies, SRS3D Headphone and SRS3D extreme mode. SRS3D Headphone is 3D surround technology optimized for headphones, SRS3D extreme mode is optimized for small speakers mounted in close proximity.

To disable 3D surround, LSI support “Bypass mode”.

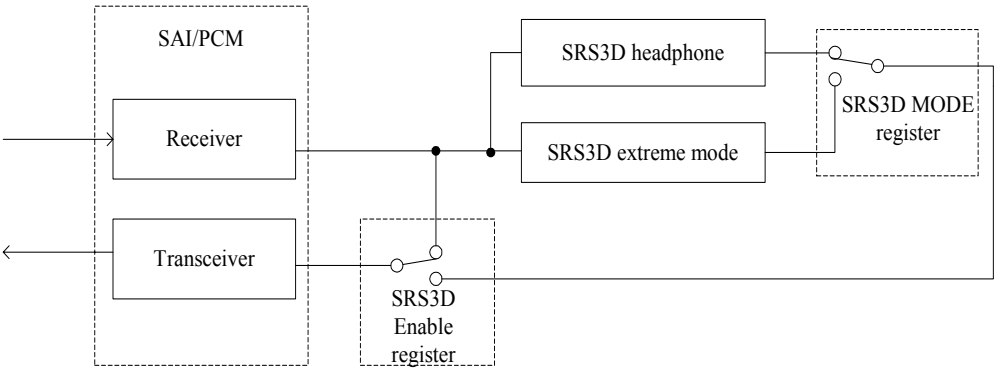


Fig.16 3D Function Diagram

NOTICES for 3D surround

The strength of 3D surround effect is selectable by register values. As there is only one parameter in each mode, the strength is easily changed.

When the 3D surround is enabled please consider the sound volume. If the input volume to the LSI is high, the output with the 3D surround effect might be distorted. In such case, please reduce the audio gain before inputting to the LSI. Regarding the attenuation value, please determine it by system evaluation.

Set 3D Surround

It needs to set the Sampling Frequency Register Setting before processing the PCM signal. Before changing the value of the register, please turn off the 3D effect by setting SRS3D Enable register.

The strength of 3D effect can be adjusted by the corresponding controlling registers in a different mode.

These parameters can be changed anytime even if the 3D effect is on.

- Related register
  - SRS3D Enable register
  - Sampling Frequency setting register
  - SRS3D Mode register
  - SRS3D Stereo Control register
  - SRS3D Extreme mode control register

Power Down

Power Down function can reduce the power consumption.

- Power Down

Stopping the ML2601 on-board clock will stop the LSI's Digital function and power down the LSI. Inputting a "H" signal on the CLKPD pin will stop the on-board clock and power down the LSI. The I2C and SAI/PCM interface will not operate during LSI power down.

However, all the register settings will be kept during LSI power down.

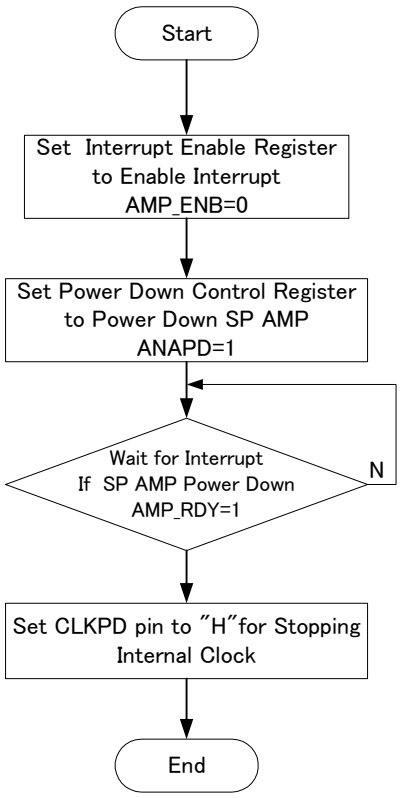


Fig.17 LSI Power Down Flow

During Power Down the ML2601's amplifier will only continue working if the power down sequence above is followed. In this case, input "H" on the CLKPD Pin. Please note, as I2C cannot communicate during Power Down, the volume and power down/on control of the speaker amplifier cannot be changed by commands sent from the CPU.

- Release Power Down

The LSI's on-board clock will begin to operate when inputting "L" on CLKPD Pin. This will release LSI from power down.
When the input clock amplitude to the ML2601 is small, there is a settling period from inputting "L" on CLKPD Pin to when the on-board clock is stable. (Please refer to the information in the Clock chapter). Accessing the LSI during this period is invalid.

During initialisation of the ML2601, please set the Clock Feedback Resistor Register according to the amplitude of the input clock after inputting "L" on CLKPD Pin and the stable period of the on-board clock.

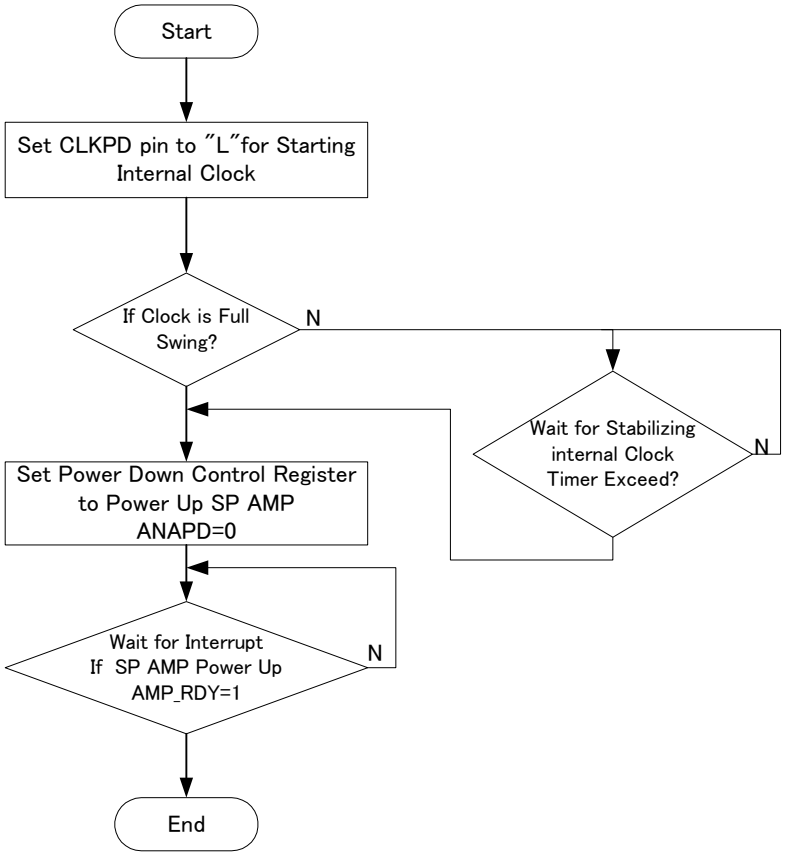


Fig.18 Release Power DownFlow

- Power Down Amplifier

The ML2601 amplifier can be powered down by setting the Power Down Control Register. An interrupt signal will be sent by the ML2601 once the on-board Amplifier has powered down and then powered on.

Please refer to the Fig.17 for the information about the interrupt signal action and the Amplifier action when power down / Power on.

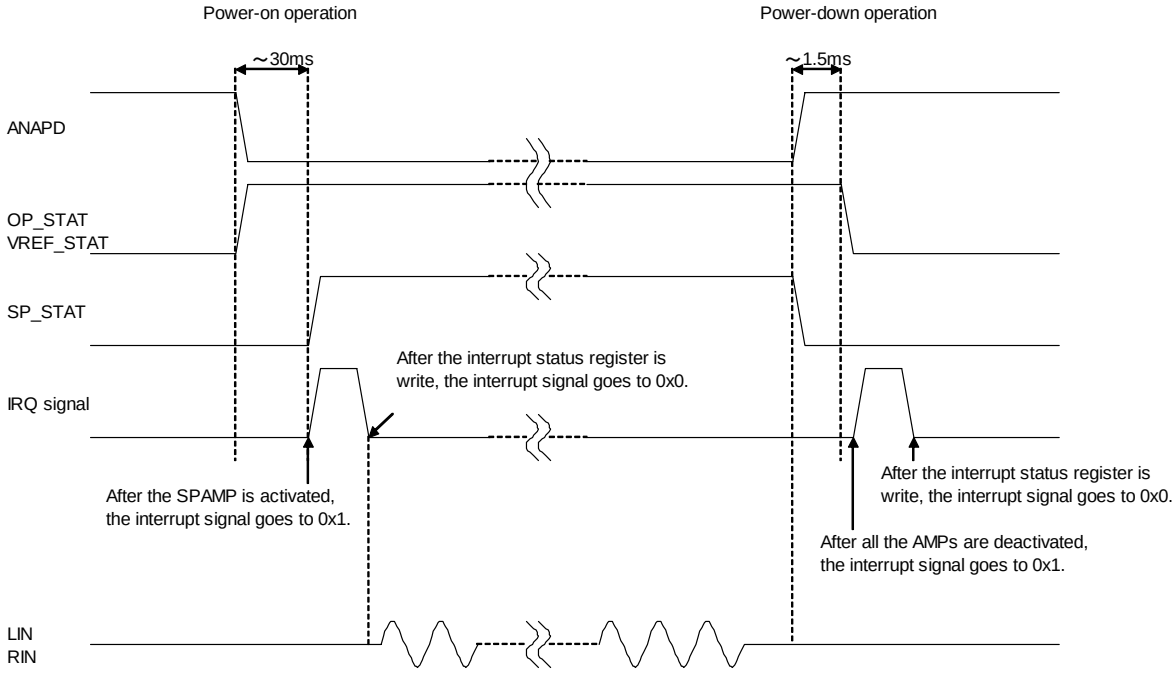


Fig.19 Power On/Down Amplifier Sequence

In order to avoid pop-noise when in power down ML2601, please set ANAPD bit to “1” and stop the input source after the interrupt has occurred.

In order to avoid pop-noise when releasing power down, please start the analog source signal before setting ANAPD bit to “0”. Input the signal after the interrupt occurred.

Note
The polarity of the interrupt signal can be changed by the ISS bit in the Interrupt Polarity Control register.

- Related register
  Power Down Control register
  Interrupt Status register
  Interrupt Enable register
  Analog Status register
  Interrupt Polarity Control register

Register Map

Address	Access	B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00	Note
Clock, Reset , Power down Control Register																		
0x0004	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	DIVSEL 0	Clock select
0x0008	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	RFOFF 0	Clock feedback resistor control
0x0016	R/W															PCMPD 1	ANAPD 1	Power down control
0x0020	W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	SOFTRST -	Soft reset
3D Control Register																		
0x0102	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	SRS3DEN 0	SRS3D enable
0x01b0	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	XTMode 0	SRS3D mode
0x01b2	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	SCN6 1	SCN5 1	SCN4 0	SCN3 0	SCN2 1	SCN1 1	SCN0 0	SRS3D stereo control
0x01b4	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	ECN6 1	ECN5 1	ECN4 0	ECN3 0	ECN2 1	ECN1 1	ECN0 0	SRS3D extreme mode control
0x01b6	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	FRQ2 0	FRQ1 1	FRQ0 0	Sampling frequency setting
PCM I/F Control Register																		
0x0100	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	SAI 0	SAI/PCM interface select
SAI I/F Control Register																		
0x0190	R/W	- -	- -	- -	- -	- -	- -	- -	- -	DLY1 0	- -	- -	- -	- -	- -	DLY0 0	WSL 0	SAI control
Analog Control Register																		
0x0116	R/W	- -	- -	- -	- -	SPVLL3 0	SPVLL2 0	SPVLL1 0	SPVLL0 0	- -				SPVLR3 0	SPVLR2 0	SPVLR1 0	SPVLR0 0	Speaker amplifier volume control
0x0118	R	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	SP_STAT 0	OP_STAT 0	VREF_STAT 0	Analog status
Interrupt Control Register																		
0x0010	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	AMP_RDY 0	Interrupt status
0x0012	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	AMP_ENB 0	Interrupt enable

0x0014	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	ISS 1	Interrupt polarity control
PCM Slave Control Register																		
0x0200	R/W	- -	- -	- -	- -	- -	- -	- -	- -	SSLI7 1	SSLI6 1	SSLI5 1	SSLI4 1	SSLI3 1	SSLI2 1	SSLI1 1	SSLI0 1	Left channel input slot start
0x0202	R/W	- -	- -	- -	- -	- -	- -	- -	- -	SSRI7 1	SSRI6 1	SSRI5 1	SSRI4 1	SSRI3 1	SSRI2 1	SSRI1 1	SSRI0 1	Right channel input slot start
0x0204	R/W	- -	- -	- -	- -	- -	- -	- -	- -	SSLO7 1	SSLO6 1	SSLO5 1	SSLO4 1	SSLO3 1	SSLO2 1	SSLO1 1	SSLO0 1	Left channel output slot start
0x0206	R/W	- -	- -	- -	- -	- -	- -	- -	- -	SSRO7 1	SSRO6 1	SSRO5 1	SSRO4 1	SSRO3 1	SSRO2 1	SSRO1 1	SSRO0 1	Right channel output slot start
0x0208	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	ISL 0	ISR 1	OSL 0	OSR 1	Channel Select
0x020A	R/W	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	BOOR 0	BOOL 0	BOIR 0	BOIL 0	Bit Order

Detailed Description of the Registers System Control

Note: "-" indicates a reserved bit. They return "0" for reads. Always write "0" to the bit. If a"1"is written to this bit, the operations cannot be guaranteed.

CLOCK select register (Address 0x0004; Access R/W)

Clock, Reset , Power down Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	DIVSEL 0

This register controls the division circuit for input clock.

DIVSEL bit: It switches ON or OFF for dividing input clock.

When a 26MHz clock is inputted to the CLOCK, this register must be set to "1". This clock is then divided down to 13MHz and is used as internal system clock. The internal system clock must be set as 13MHz.

DIVSEL	Description
"0"	Input clock signal into CLOCK pin is used directly for the internal system clock. The division circuit is skipped.(default)
"1"	Input clock signal into CLOCK pin is divided down to 13MHz through the division circuit. This is used for the internal system clock.

Clock Feedback Resistor Control Register (Address 0x0008; Access R/W)

Clock, Reset , Power down Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	RFOFF 0

This register controls the feedback resistor for the clock buffer of the CLOCK pin.

RFOFF bit: It switches ON/OFF for feedback resistor of the clock buffer.
For a full swing clock, set this register to “1” which disables the feedback resistor. The current consumption is reduced.

RFOFF	Description
“0”	The feedback resistor is valid. A small amplitude clock is acceptable.(default)
“1”	The feedback resistor is invalid. Full swing clock must be inputted.

Power Down Control Register (Address 0x0016; Access R/W)

Clock, Reset , Power down Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	PCMPD 1	ANAPD 1

This register controls power down of the LSI。

ANAPD: controls power down/on of the on-board amplifier.
To power down the amplifiers, set ANAPD bit to “1”. The current consumption will be reduced.

ANAPD	Description
“0”	Power on SP-AMP
“1”	Power down SP-AMP

PCMPD: Controls power down/on of the PCM interface
To power down the PCM interface, set PCMPD bit to “1”. The current consumption will be reduced.

PCMPD	Description
“0”	Power on PCM interface
“1”	Power down PCM interface

Software Reset Register (Address 0x0020; Access W)

Clock, Reset , Power down Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	SOFTRST

This register is for reset all.

SOFTRST bit: When it is set to “1”, all the registers are reset to the default setting.

NOTICE: When a software reset is performed while the speaker amp is active you may experience a pop noise.

SRS3D Enable Register (Address 0x0102; Access R/W)

3D Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	SRS3DEN 0

This register is to enable or disable the SRS3D effect

SRS3DEN bit: This bit is to enable or disable the SRS3D effect. When SRS3D is disabled, PCM data from SAI/PCM will bypass the SRS3D block, the data is outputted from the LSI through the SAI/PCM interface.

SRS3DEN	Description
"0"	SRS3D effect is disabled
"1"	SRS3D effect is enabled

Sampling Frequency setting register (Address 0x01b6; Access R/W)

3D Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	FRQ2 0	FRQ1 1	FRQ0 0

This register is to set the sampling frequency of the 3D surround effect.
When changing the register, please disable the SRS3D effect.

FRQ[2:0]bit: Please set sampling frequency according to the PCM data. An incorrectly matched sampling frequency will affect optimal effect performance.

FRQ[2:0]	Description
0x0	reserved *
0x1	reserved *
0x2	16 kHz
0x3	22.05 kHz
0x4	24 kHz
0x5	32 kHz
0x6	44.1 kHz
0x7	48 kHz

*** Overwriting for "*reserved" bit is prohibited, no guarantee of proper operation.**

SRS3D Mode Register (Address 0x01b0; Access R/W)

3D Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	SRS3DMODE 0

This register is to set SRS3D mode

SRS3DMODE bit: This bit is to set SRS3D mode。
Please disable the SRS3D effect before change this bit.

SRS3DMODE	Description
“0”	SRS3D Headphone mode
“1”	SRS3D Extreme mode(For speaker)

SRS 3D Stereo Control Register (Address 0x01b2; Access R/W)

3D Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	- -	- -	- -	- -	- -	SCN6 1	SCN5 1	SCN4 0	SCN3 0	SCN2 1	SCN1 1	SCN0 0

This register is to set the strength value of the SRS3D headphone mode.

SCN[6:0]: The bits to set 3D strength value of the SRS3D headphone mode. The value can be set from 0x00 to 0x7F.

SRS 3D Extreme mode Control Register (Address 0x01b4; Access R/W)

3D Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	- -	- -	- -	- -	- -	ECN6 1	ECN5 1	ECN4 0	ECN3 0	ECN2 1	ECN1 1	ECN0 0

This register is to set the strength value of the SRS3D Extreme mode (for speaker).

ECN[6:0]: The bits to set 3D strength value of the SRS3D Extreme mode. The value can be set from 0x00 to 0x7F.

SAI/PCM Interface Select Register (Address 0x0100; Access R/W)

PCM I/F Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	SAI 0

This register is to select the PCM interface between SAI and PCM.

SAI bit:。This bit to select the PCM interface, either SAI or PCM.

SAI	Description
0	PCM interface is selected(default)
1	SAI interface is selected

***This register must not be set during PCM data transmission, or no guarantee of proper operation.**

Left Channel Input Slot Start Register (Address 0x0200; Access R/W)

PCM Slave Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	- -	- -	- -	- -	SSLI7 1	SSLI6 1	SSLI5 1	SSLI4 1	SSLI3 1	SSLI2 1	SSLI1 1	SSLI0 1

The value of this register is the number of PCM_CLK cycles. After SSLI cycles since PCM_SYNC positive edge, the slot for left channel data input starts. The four slot start registers must be set to values which do not allow the slots to overlap.

Right Channel Input Slot Start Register (Address 0x0202; Access R/W)

PCM Slave Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	- -	- -	- -	- -	SSRI7 1	SSRI6 1	SSRI5 1	SSRI4 1	SSRI3 1	SSRI2 1	SSRI1 1	SSRI0 1

The value of this register is the number of PCM_CLK cycles. After SSRI cycles since PCM_SYNC positive edge, the slot for right channel data input starts. The four slot start registers must be set to values which do not allow the slots to overlap.

Left Channel Output Slot Start Register (Address 0x0204; Access R/W)

PCM Slave Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	- -	- -	- -	- -	SSLO7 1	SSLO6 1	SSLO5 1	SSLO4 1	SSLO3 1	SSLO2 1	SSLO1 1	SSLO0 1

The value of this register is the number of PCM_CLK cycles. After SSLO cycles since PCM_SYNC positive edge, the slot for left channel data onput starts. The four slot start registers must be set to values which do not allow the slots to overlap.

Right Channel Output Slot Start Register (Address 0x0206; Access R/W)

PCM Slave Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
--	--	--	--	--	--	--	--	SSRO71	SSRO61	SSRO51	SSRO41	SSRO31	SSRO21	SSRO11	SSRO01

The value of this register is the number of PCM_CLK cycles. After SSRO cycles since PCM_SYNC positive edge, the slot for right channel data output starts. The four slot start registers must be set to values which do not allow the slots to overlap.

Channel Select Register (Address 0x0208; Access R/W)

PCM Slave Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	ISL 0	ISR 1	OSL 0	OSR 1

This Register controls the I/O terminal of the PCM data when the "PCM interface" is used.

The I/O terminal for data of the Left-Channel and Right-Channel is selected by this Register.

*This Register is effective only when the "PCM interface" is selected by "PCMIF_Ctrl" register.

ISL bit: This bit is to set the Input terminal of the Left-Channel.
Please disable the PCM Interface before changing this bit.

ISL	Description
"0"	Left-channel input from PCM_DATA1 (default)
"1"	Left-channel input from PCM_DATA2

ISR bit: This bit is to set the Input terminal of the Right-Channel.
Please disable the PCM Interface before changing this bit.

ISR	Description
"0"	Right-channel input from PCM_DATA1
"1"	Right-channel input from PCM_DATA2 (default)

OSL bit: This bit is to set the Output terminal of the Left-Channel.
Please disable the PCM Interface before changing this bit.

OSL	Description
"0"	Left-channel output to PCM_DATA1 (default)
"1"	Left-channel output to PCM_DATA2

OSR bit: This bit is to set the Output terminal of the Right-Channel.
Please disable the PCM Interface before changing this bit.

OSR	Description
"0"	Right-channel output to PCM_DATA1
"1"	Right-channel output to PCM_DATA2 (default)

Bit Order Register (Address 0x020A; Access R/W)

PCM Slave Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	BOOR 0	BOOL 0	BOIR 0	BOIL 0

The Bit order for each channel can be selected between MSB-first and LSB-first by utilising the four bits BOIL, BOIR, BOOL and BOOR.

This device can support two kind of PCM data (16-bit PCM and 8-bit PCM). When 8-bit PCM data is employed, it is necessary to fix the lower 8-bits to "0". Table 1 shows the data format that can be supported.

The relationship between bit order of data and the Bit Order Register is shown in table 2.

Table 1: Supported PCM data format

Kind of PCM data	B15	……	B8	B7	……	B0
16-bit PCM	MSB	……				LSB
8-bit PCM	MSB	……	LSB	0	……	0

Table 2: MSB-first or LSB-first vs. Bit Order Register

PCM Data		Set Value of "Bit Order" Register (BOOR, BOOL, BOIR, BOIL)	Receive data or transmission data on PCM bus (PCM_DATA1 or PCM_DATA2)					
Bit width	Bit Order		First bit					Last bit
			B0	……	B7	B8	……	B15
16bit PCM	MSB-First	1	MSB	……				LSB
	LSB-First	0	LSB	……				MSB
8bit PCM	MSB-First	1	MSB	……	LSB	0	……	0
	LSB-First	0	0	……	0	LSB	……	MSB

SAI Control Register (Address 0x0190; Access R/W)

SAI I/F Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	- -	- -	- -	- -	DLY1 0	- -	- -	- -	- -	- -	DLY0 0	WSL 0

This register is to set the format of the SAI. Please don't change this register during operation of the SAI.

WSL bit: This bit is to set the polarity of SAI_LRCLK.

WSL	Description
0	LEFT channel is operating when SAI_LRCLK is L level. (default)
1	LEFT channel is operating when SAI_LRCLK is H level.

DLYO bit: This bit is to specify the data output delay from the transceiver.

DLYO	Description
0	There is one clock delay in serial output data (default)
1	No delay in serial output data

DLY bit:This bit is to specify the data output delay from the receiver.

DLYI	Description
0	There is one clock delay in serial output data (default)
1	No delay in serial output data

Speaker Amplifier Volume Control Register (Address 0x0116; Access R/W)

Analog Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	SPVLL3 0	SPVLL2 0	SPVLL1 0	SPVLL0 0	- -	- -	- -	- -	SPVLR3 0	SPVLR2 0	SPVLR1 0	SPVLR0 0

This register sets the volume of the speaker amplifier. SPVLL[3:0] is to set L ch, SPVLR[3:0] is to set R ch。

SPVLL[3:0]、SPVLR[3:0] bit

SPVLL/SPVLR	Volume Gain	SPVLL/SPVLR	Volume Gain
0x0	8dB	0x8	-8dB
0x1	6dB	0x9	-10dB
0x2	4dB	0xA	-12dB
0x3	2dB	0xB	-14dB
0x4	0dB	0xC	-16dB
0x5	-2dB	0xD	-18dB
0x6	-4dB	0xE	-20dB
0x7	-6dB	0xF	MUTE

Analog Status Register(Address 0x0118; Access R)

Analog Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	SP_STAT 0	OP_STAT 0	VREF_STAT 0

This register is to indicate the status of the on-board stereo speaker amplifier. Each bit will be set as "1" when the related amplifier is ON.

SP_STAT bit: This bit is to indicate the status of the speaker amplifier.

SP_STAT	Description
0	Amplifier OFF (default)
1	Amplifier ON

OP_STAT bit: This bit is to indicate the status of the volume block.

OP_STAT	Description
0	Amplifier OFF (default)
1	Amplifier ON

VREF_STAT bit: This bit is to indicate the status of the VREF block

VREF_STAT	Description
0	Amplifier OFF (default)
1	Amplifier ON

Interrupt Status Register (Address 0x0010; Access R/W)

Interrupt Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	AMP_RDY 0

This register is to indicate the interrupt status. IRQ can be cleared by writing a ”1” to the AMP_RDY bit. This register is available even if the interrupt is disabled through the interrupt enable register.

AMP-RDY bit: This bit will be set to ”1” when the status of SP_STAT bit (speaker amplifier) equals the status of the ANAPD bit (Analog Power Down).
The interrupt can be cleared by writing a ”1” to this bit.

AMP_RDY	Description
0	Not interrupt (default)
1	Interrupt occurred

Interrupt Enable Register (Address 0x0012; Access R/W)

Interrupt Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	AMP_ENB 0

This register is to enable or disable the interrupt.

AMPENB bit: This bit is to be enable or disable the interrupt.

AMP_ENB	Description
“0”	Disenable the interrupt (default)
“1”	Enable the interrupt

Interrupt Polarity Control Register (Address 0x0014; Access R/W)

Interrupt Control Register															
B15 (Initial)	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00
- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	- -	ISS 1

This register is to set the polarity of the interrupt.

ISS bit: This bit is to set the polarity of the interrupt.

ISS	Description
“0”	IRQ is "L" activity
“1”	IRQ is "H" activity (default)

Revision History

Date	Page	Notes	Revision
05/11/07	All	Release first version	1.0.0
05/11/29	14	Correct PCM timing and parameter values	1.0.1
05/11/29	27,28	Modify note of register map	1.0.1
05/11/29	29-50	Delete symbol name of register	1.0.1
05/11/29	8	Correct note	1.0.1
05/11/29	8-17	Correct centigrade symbol	1.0.1
05/11/29	Top page	Add SRS Labs trademark usage	1.0.1
05/12/27	8,10,13,14,17	Modify name of the signal and delete TBD item	2.0.0
05/12/27	18	Update the Power Derating Curves	2.0.0

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